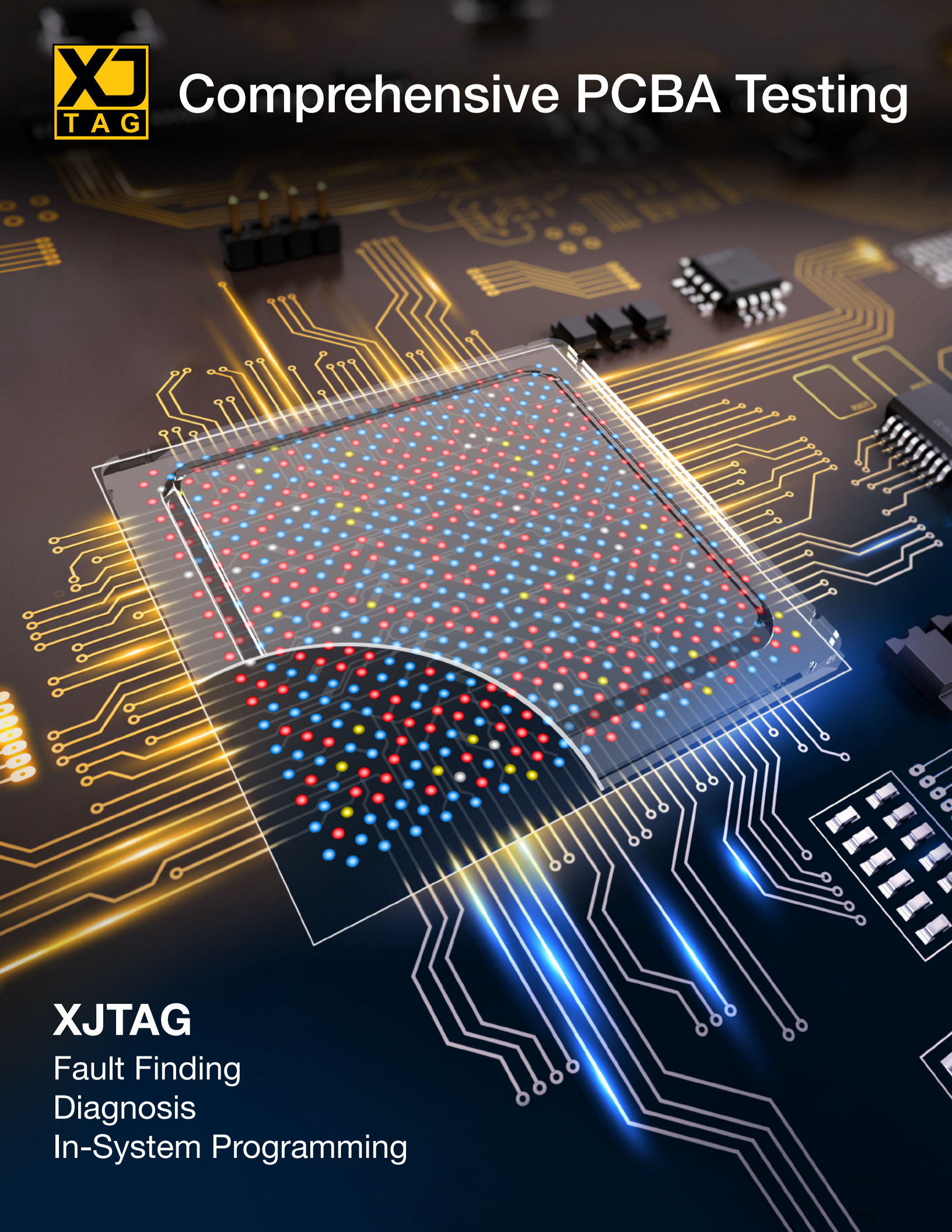
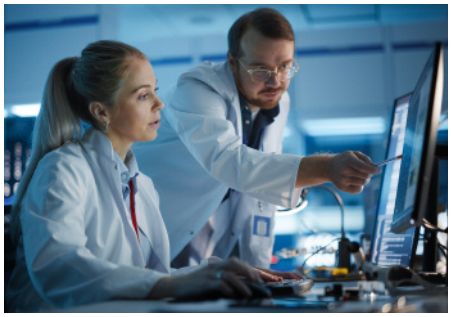
Comprehensive PCBA Testing



XJTAG

Fault Finding
Diagnosis
In-System Programming

XJTAG Boundary-Scan Software

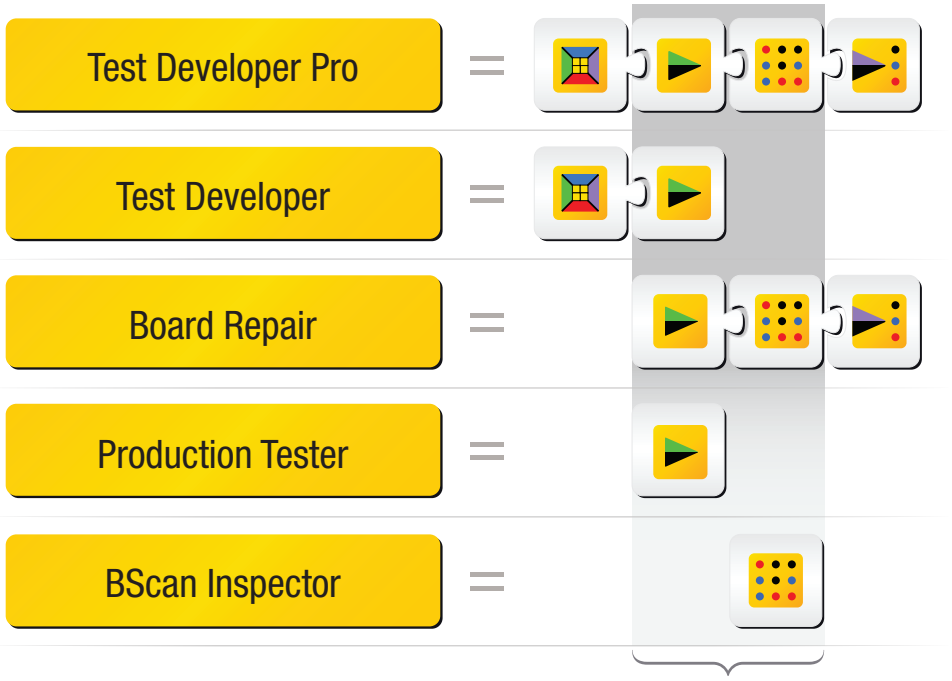


XJTAG offers a range of software packages to meet your company's needs.

Test Developer Pro contains XJTAG's full suite of boundary scan applications – XJDeveloper, XJInvestigator, XJRunner and XJAnalyser.

Test Developer Pro + XJIO has all these software applications plus an XJIO board. This allows you to improve coverage by testing all the way through the connectors on your board.

Select your software package



Standalone versions of XJRunner and/or XJAnalyser are also included with your integrated environment's license

XJDeveloper

Test and Programming Development & Debug Environment

XJDeveloper's intuitive IDE makes it quick and easy to set up your tests for a circuit board.

An automatically generated connection test will check for short circuit faults between accessible nets, stuck-at faults, pull resistor faults and some open circuit faults.

You can add further test coverage by using the built-in library of test models to interact with non-JTAG devices such as Flash, RAM, Ethernet, A/D, Logic, I²C, SPI, PCI, etc.

Tests can be set up as soon as board design is complete, and a test coverage report produced. This process highlights certain design issues when they are still easily fixed, before building prototypes.

The integrated XJRunner allows you to run the full test system during board bring-up. A standalone XJRunner license is also included so you can test deployment before sending to production.

XJInvestigator

Manufacturing Repair/Rework Station

Much more than a production line test tool, XJInvestigator is a repair focused, integrated test and debug environment for fault analysis, helping you efficiently recover failing boards.

XJInvestigator has all of the features of XJRunner and XJAnalyser plus extra debug features from XJDeveloper (see the XJInvestigator product sheet for more details).

XJAnalyser

Prototype Board Bring-up & Real-time Graphical Board Debug

Using the graphical interface you can interact with devices in your JTAG chain to debug your boards. You simply click on a pin to control its state – no code required.

XJRunner

Run-time Manufacturing Test & Programming Environment

XJRunner allows you to execute XJDeveloper tests. Provides high precision fault information, including integrated Layout and Schematic Viewers, to help you with easy fault-finding.

Privilege levels ensure that users see a suitable interface, and can prevent tests being skipped. Log files are produced for audit/QA purposes.

You can use XJRunner for parallel testing and programming using auxiliary controllers or an XJQuad.

JTAG Chain Debugger

Helps you troubleshoot a faulty JTAG chain. Checks JTAG signal integrity, calculates max. JTAG clock speed. Included with all packages.

XJFlash

Using the optional XJFlash module you can improve flash programming speeds up to 50-fold with certain flash/FPGA configurations.

XJTAG Boundary-Scan Hardware

Select your hardware features

XJTAG is easy to use on multiple machines. Licenses are not locked to a PC; they can be stored in the hardware interface or taken from a network license server, while any of these portable hardware options allow you to connect your computer with your circuit.

Hardware features		Frequency measurements	Voltage banks	Voltage measurements	Number of JTAG controllers	TAPs per JTAG controller	GPIO on pins	TCK frequencies up to (MHz)	Connection
XJLink2	Benchtop development and test	✓	✓	✓	1	4	✓	166	USB
XJQuad	Production	✓	✓	✓	4	4	✓	166	USB
PXI-XJLink2	LabVIEW integration	✓	✓	✓	1	4	✓	166	PXI
XJLink2-3030	High volume / test integration	✓	✓	✓	1	4	✓	166	SPEA 3030
XJLink2-3070	High volume / test integration	✓	✓	✓	1	4	✓	166	Keysight Utility Card
XJLink2-CFM	High volume / test integration	✓	✓	✓	1	4	✓	166	Teradyne TestStation

XJLink2

XJLink2 is an enhanced, portable USB JTAG controller with configurable pin-out.

The small, lightweight design means an XJLink2 can easily be taken to the Unit Under Test (UUT), while a number of advanced features make it easy to connect to a wide range of circuit boards.

XJQuad

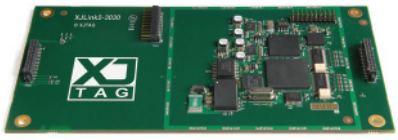
XJQuad is a 4-port version of the XJLink2 USB-to-JTAG controller. It is particularly suitable for volume production testing.

XJQuad can be used for testing four boards simultaneously or independently. It is supplied with XJRunner software.

PXI-XJLink2

PXI-XJLink2 allows you to easily use XJTAG in PXI-based test systems.

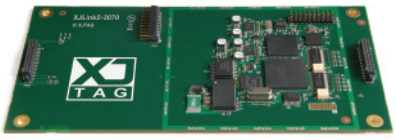
A full set of integration interfaces and examples are installed with XJTAG to allow easy integration into test executives such as LabVIEW™ and LabWindows™ or bespoke .NET applications.



XJLink2-3030

XJLink2-3030, approved by SPEA, allows you to easily use XJTAG in SPEA 3030™ ICT bed-of-nails board testers.

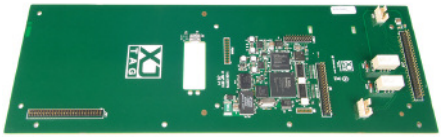
It fits into one slot on the SPEA 3030 XJLink2 Carrier Board and is fully integrated into the SPEA Leonardo environment.



XJLink2-3070

XJLink2-3070, approved by Keysight Technologies, allows you to easily use XJTAG in Keysight i3070™ ICT machines.

It fits into one slot on the Keysight (Agilent) i3070 utility card and is fully integrated into the BTBasic environment.



XJLink2-CFM

XJLink2-CFM allows you to easily use XJTAG in Teradyne TestStation™ ICT machines.

XJLink2-CFM fits into one slot on the Teradyne Multi-Function Application Board.

XJIO is a test expansion board with 208 digital I/Os, 8 ADC, 8 DAC, RS232 / UART, buttons and LEDs. It allows you to improve fault isolation, verify power rail levels, and replace costly custom test jigs – even for non-JTAG boards.

Seven reasons why you should use XJTAG to test your boards

Three simple letters – BGA

An increasing number of devices are supplied in Ball Grid Array (BGA) packaging. Each BGA device on a board imposes severe restrictions on the testing that can be done using traditional bed-of-nails or flying probe machines.

Using a simple four-pin interface, JTAG boundary scan allows the signals on enabled devices to be controlled and monitored without any direct physical access.

Lower test development / NRE costs

As different processors and FPGAs interact with peripherals in different ways, traditional functional test requires costly custom development for each board. JTAG boundary scan significantly reduces such development costs because it provides a simplified interface to control the I/O pins used for peripheral interactions. This standard interface is the same for all JTAG-enabled devices, allowing the use of a generic set of reusable test models when building test systems.

The non-recurring engineering (NRE) expenses of building test fixtures can be prohibitively high. In many cases, using JTAG boundary scan will remove the need for such a fixture, in other cases the fixture can be dramatically simplified resulting in significant cost savings.

Shorter test times

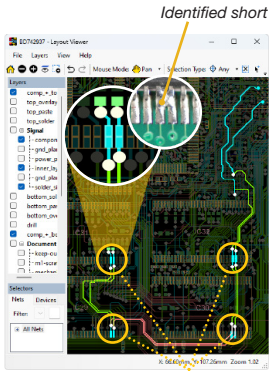
For boards with low production volumes it has always been difficult to justify the cost of test fixture development. Flying probe testing can be one alternative, however, the test cycle times tend to be high. JTAG boundary scan testing gives fast test times with no need for a costly fixture.

Production-level benchtop tests for prototypes

Traditional test technologies require very large and expensive equipment. The only test equipment required for JTAG boundary scan testing is a JTAG controller – XJTAG's XJLink2 controller is a similar size to a PC mouse.

Excellent fault diagnostics

JTAG boundary scan, unlike functional test, provides high precision fault information to help with rapid repair. XJTAG also provides the capability to view both the physical location of a fault on the layout of the board and the logical design of the area of the circuit in which the fault exists on the schematic.



Most likely short locations

One tool for test and programming

JTAG is often already used as one step in production: programming. By also using JTAG for boundary scan test it is possible to reduce the number of steps and handling operations in the production process.

Recover boards that are 'dead' to functional test

XJTAG boundary scan tests can be run on any board with a working JTAG interface. Traditional functional tests cannot be run if the board does not boot; simple faults on key peripherals, such as RAM or clocks, would be found using JTAG but would prevent functional tests from providing any diagnostic information.

"XJTAG offers incredible power, performance and versatility..."

ARM – Andy Evans, Sr Product Engineer, Platforms, Development Systems

"We selected the XJTAG system due to its price, the speed and accuracy of fault diagnosis..."

Curtiss-Wright – Alan McCormick, MD, Video and Graphics Group

"XJTAG has features that are vastly superior to other systems I know..."

Eaton – James Diem, Test Engineering Manager

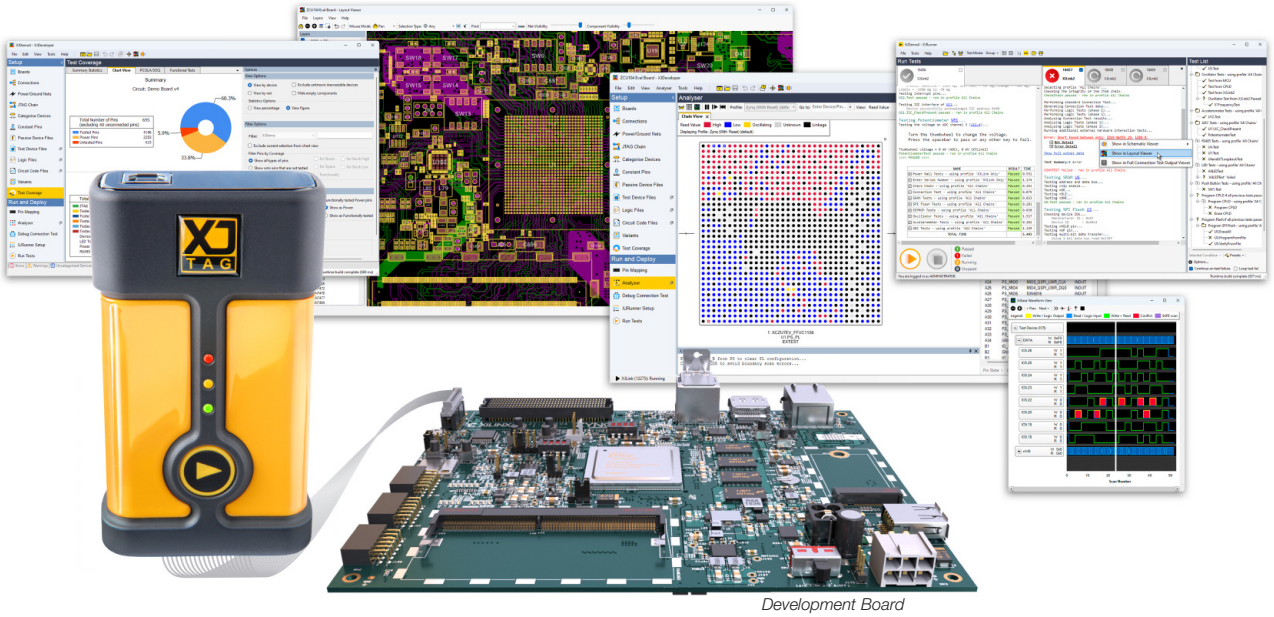
"XJTAG is easy to use, highly effective and flexible... The reuse of tests is a big time-saver."

Saab – Eduard Stander, Controllers Group, Electronic Defence Systems

XJTAG-SUMM-24E-02

Special Offer

Free Board Setup + Free XJTAG Trial



Development Board

- Do you design boards with BGAs on?
- Does your hardware include FPGAs, CPLDs, DSPs or microprocessors?
- Would you like to debug your boards, detect faults and prove your design quickly and easily?

Well, this is where **XJTAG Boundary Scan can help** by offering you a **FREE 30-day trial of XJTAG on your own board**.

Yes, that's right, XJTAG will set up its test system on your board for free when you take a 30-day trial.

Apply today and discover how XJTAG can help you save time and money

Find out why leading companies are using XJTAG

"XJTAG is an absolute necessity for any company designing complex circuits that feature high pin count BGA or chip scale devices."

"XJTAG is easy to use and incredibly fast, which has enabled us to shave weeks off the development schedule for our RFeye module thereby freeing our development team from time-consuming debugging tasks."

Alistair Massarella, CEO – **CRFS**

ARM Case Study

ARM selects XJTAG for RealView development tools debug and test

ARM, the world's leading semiconductor intellectual property (IP) supplier, has reduced the time and cost of developing its range of RealView® development tools by using the XJTAG boundary scan development system to improve and speed up the process of debugging and testing its high density, multi-layer development boards.

Apply now

www.xjtag.com/trial



Saab Cuts Costs and Boosts Productivity with XJTAG® Boundary Scan

"Defense and Security company Saab selected the XJTAG development system to speed up the process of debugging and testing multi-layer development boards destined for its IDAS and CIDAS projects used in electronic warfare systems."

Saab serves the global market with world-leading solutions, products and services ranging from military defense to civil security. With operations and employees on every continent, Saab continuously develops, adapts and improves new technology to meet customers' changing needs. Saab operates in five business areas: Aeronautics, Dynamics, Electronic Defense Systems, Security and Defense Solutions, and Support and Services.

The versatility of the XJTAG system made it an attractive choice for world-leading defense and security specialist Saab, which needed a reliable test solution to test multi-layer development boards destined for airborne and naval electronic warfare systems used in its IDAS and CIDAS products.

"We have initially used XJTAG in the production environment to test our complex, high density, multi-layered board designs containing FPGAs and CPLDs, and have recently introduced the solution to the development and debug stage with great success," says Eduard Stander, who works for the Controllers Group at Saab's Electronic Defense Systems, South Africa.

"Using XJAnalyser has allowed us to reduce initial debug issues, and to debug errors in a shorter time than our existing tools allowed us."

"We have found that using the XJTAG solution, and the Layout Viewer in particular, has quantifiably reduced the cost of developing product test jigs in our production test department, because of the fast and accurate diagnosis the system provides."

"We now can test products that have processors, SDRAM and FLASH memories, Ethernet PHYs, A/D Converters, real time clocks, serial ports, voltage regulators."

The team at Saab opted for XJTAG because of its superior cost-to-performance ratio and, like many of XJTAG's customers, they were particularly impressed with the flexibility of the system.

XJTAG makes it easy to write test routines for devices and allows users to store them in a library so they can be reused again when the same, or a similar component, is used.

The XJTAG Professional System provides an extensive library of reusable scripts while XJEase, XJTAG's high-level test description language, allows engineers to write and customize tests for JTAG and non-JTAG components without needing to understand how boundary scan works. These tests can be re-used throughout the product lifecycle as well as in subsequent projects wherever the same component is used.

"The reuse of tests on the XJTAG system is a big time saver," says Eduard. "The design for test (DFT) reports help us ensure that a very high percentage of our circuits are testable before we go into serial production and, with the aid of boundary scan tests, we get closer to our goal of 100% test coverage on production Shop Replaceable Units (SRU)."

He adds: "XJTAG's high-level test description language XJEase is central to this flexibility. The ability to design low level test with XJEase is a real advantage as the test scripts let you drive the non-JTAG components directly."

Eduard says the company's next step is to integrate XJTAG's portable boundary scan oscilloscope product – XJTAG Expert – with its functional test equipment. "XJTAG is easy to use, highly effective and flexible enough to evolve with our test strategies as we focus on improving speed and productivity."

opinion

Eduard Stander
Controllers Group
Saab

"The reuse of tests on the XJTAG system is a big time saver. The design for test (DFT) reports help us ensure that a very high percentage of our circuits are testable before we go into serial production and, with the aid of boundary scan tests, we get closer to our goal of 100% test coverage on production Shop Replaceable Units (SRU)."

"We have initially used XJTAG in the production environment to test our complex, high density, multi-layered board designs containing FPGAs and CPLDs, and have recently introduced the solution to the development and debug stage with great success."

SAAB

Company	Saab HQ Sweden
Nature of business	Defense and security solutions
Customers	Global market with world-leading products, services and solutions from military defense to civil security
Locations	Operations on every continent
Employees	13,000
Revenue	SEK 23,5 billion 20% related to R&D
Web site	www.saabgroup.com

Andy Evans, Senior Product Engineer at ARM

ARM Selects XJTAG® for Debug and Test of its RealView Development Tools

"ARM, the world's leading semiconductor intellectual property (IP) supplier, has reduced the time and cost of developing its range of RealView development tools by using the XJTAG boundary scan development system to improve and speed up the process of debugging and testing its high density, multi-layer development boards."

ARM® technology lies at the heart of advanced digital products from mobile, home and enterprise solutions to embedded and emerging applications. ARM's comprehensive product offering includes 16/32-bit RISC microprocessors, data engines, graphics processors, digital libraries, embedded memories, peripherals, software and development tools, as well as analogue functions and high-speed connectivity products.

To support the company's SoC IP, ARM has developed a strong base of development tools, software and hardware products. For example, its range of RealView® development solutions are ideal systems for customers prototyping ARM processor-based products and are suitable for architecture and CPU evaluation, hardware and software design, and ASIC emulation. These development platforms are typically highly complex, high density, twelve-to-sixteen layer board designs, containing multiple high pin-count ball grid array (BGA) devices including processors, ASICs, FPGAs and CPLDs.

"Our development platforms are used extensively across the business and are designed to deliver significant risk reduction and faster time-to-market benefits to our Partners," said Spencer Saunders, Engineering Manager, Platforms, Development Systems, ARM.

"With tens of thousands of pins on each board, we recognized that it would not be possible to validate these circuits in a commercially realistic timescale without the use of a boundary scan test system."

After evaluating the different competitive options, the engineering team at ARM's development facility in Cambridge, UK, selected the XJTAG boundary scan development system. The XJTAG system has enabled ARM to speed up the process of debug and test, get test coverage up to around the 90 percent mark and to significantly improve production yields.

"XJTAG offers incredible power, performance and versatility and can test both boundary scan (JTAG) and cluster (non-JTAG) devices including BGA and chip scale packages," said Andy Evans, Senior Product Engineer, Platforms, Development Systems, ARM.

"XJTAG is easy to use, the test scripts for non-JTAG devices follow the familiar top-down design flow, and these test scripts are device-centric, making them re-usable from project to project, which saves ARM an awful lot of time."

ARM is currently using XJTAG on its latest generation of RealView platform baseboards, and, because of its built-in design-for-test (DFT) functionality, it has been used right from the very beginning of the design process to help improve the design and reduce respins.

"XJTAG's DFT capability is extremely powerful and saves us a great deal of time, as it automatically handles any netlist changes by adapting to the new circuit connections, thereby avoiding the time-consuming process of manually picking through the netlist for errors," said Spencer Saunders.

"In addition, XJTAG's powerful circuit visualization tool provides us with a simple graphical view of the state of all JTAG pins across the multiple BGA devices and enables us to quickly pinpoint specific faults on our boards and speed up the whole debug process."

opinion

Spencer Saunders
Engineering Manager
Platform, Development Systems
ARM

"The XJTAG boundary scan system is an extremely powerful, versatile and cost-effective product which has enabled ARM to improve and speed up the process of debugging and testing its RealView development tools. With XJTAG, we are now close to meeting our target for 90 percent test coverage and ten-minutes-per-board production test, but we also have a boundary scan system that allows tests to be recorded, refined and repeatedly re-used throughout the development cycle both by our engineering team and our contract manufacturing partners."

ARM

Company	ARM Holdings
Nature of business	World's leading semiconductor IP supplier
Main products	16/32-bit RISC microprocessors, data engines, graphics processors, digital libraries, embedded memories, software and development tools, peripherals, analogue functions and high-speed connectivity products
Locations	ARM has facilities/offices in North America, Europe, the Middle East, Far East and India
Employees	Approx. 1659
Revenues	£263.3 million (2006)
Web site	www.arm.com

Eaton

www.xjtag.com


DATA CENTERS


COMMERCIAL & INSTITUTIONAL


CONSTRUCTION


GOVERNMENT & MILITARY


RENEWABLE ENERGY & SMART GRID


ENERGY


MANUFACTURING & INDUSTRIAL


AVIATION & VEHICLES

XJTAG® Delivers Better Boundary Scan Experience for Global Technology Leader

"Familiar with the advantages of boundary scan, but frustrated by the limitations of well-known JTAG test systems, engineers at industrial-technology giant Eaton have switched to XJTAG. XJTAG is fast and easy to learn, provides convenient project setup features, allows control over test code, and enables integration with production test equipment."

Eaton is a multi-billion dollar diversified power management company with global presence and a history of innovation dating back to 1911. Today, as a leader in power management products and services, Eaton has in-house electronics competencies covering areas such as industrial controls, metering, motor protection and communications.

A test engineering team at Eaton, led by Test Engineering Manager James Diem, has over a decade of experience testing prototypes and production assemblies using boundary scan equipment. Boundary scan provides a fast and effective means of testing devices like DSPs, microprocessors, FPGAs and memories in surface-mount packages such as Ball Grid Array (BGA). "Boundary scan testing can be highly effective, especially if device pins are inaccessible, but even well-known test systems can be difficult to use and do not easily allow updating of tests or integration with a third-party test program," says James Diem.

"We found the solution to such challenges after one of our design engineers saw XJTAG being demonstrated at a trade exposition, and told us how easy it can be to create applications, generate tests, and subsequently modify test code.

"XJTAG has features that are vastly superior to other systems I know. The learning curve for new users is dramatically shorter; one training session with XJTAG gave me enough knowledge to start developing simple programs. Now, I can create a complete test for a new board in a matter of days, whereas other systems can require weeks of work. I particularly like the BOM and CAD import features, the "Categorise Devices" screen and the pin-mapping capability, which simplify initial test generation.

"Unlike other systems, XJTAG makes it easy to 'get underneath the hood' to update programs, and also provides example tests that help engineers learn how to get the best from boundary scan." James Diem also praises other features of XJTAG, such as its convenient 'floating' license, the large and growing library of tests for standard parts, and the high level of customer service provided. "When I ask questions I have complete confidence that my requests are understood and that I will receive the answers I need," he comments.

Eaton is using XJTAG for testing prototype and production assemblies. For production, XJTAG is integrated directly into systems running tests that are written in C for Virtual Instruments (CVI). The boundary scan programs are first developed using XJTAG's XJDeveloper environment and then embedded into CVI. Engineers are using XJTAG for tasks such as extending test coverage to include parts connected to the boundary scan chain such as switches, potentiometers, LEDs or logic devices, programming microprocessors in situ, and extra testing of production boards undergoing functional test.

James Diem sums up, "We have been working with XJTAG for over a year now, and I can say that it matches or exceeds the capabilities of our previous system in every respect."

opinion

James Diem
Test Engineering Manager
Eaton

"XJTAG has features that are vastly superior to other systems I know. The learning curve for new users is dramatically shorter."

"I can create a complete test for a new board in a matter of days. The BOM and CAD import features, the "Categorise Devices" screen and the pin-mapping capability simplify initial test generation. Unlike other systems, XJTAG makes it easy to 'get underneath the hood' to update programs."

"We have been working with XJTAG for over a year now, and I can say that it does everything as well as or better than our previous system."

EATON
Powering Business Worldwide

Company	Eaton, HQ Ireland
Nature of business	Global technology leader in electrical products, systems and services for energy-efficient power management
Main products	Power distribution and circuit protection; backup power protection; control and automation; lighting and security; structural solutions and wiring devices; solutions for harsh and hazardous environments; and engineering services
Customers	Industrial, commercial and residential markets worldwide
Employees	103,000 worldwide
Revenues	US$ 21.8 billion sales
Web site	www.eaton.com

Thales Selects XJTAG® for Software Radio Testing

"Thales needed a fast, extremely versatile and cost-effective boundary scan solution to debug and test complex printed circuit boards (PCBs) used in its market-leading range of software defined radios (SDRs)."

Thales' MSN 8100-H software-defined radio (SDR) platform, the first European operational software radio, has been designed as the primary component of a comprehensive high frequency communication network benefiting from the attributes of a versatile, programmable and configurable multi-channel receiver/exciter. This radio is designed for naval and ground based applications and will be used on the Royal Navy's next class of Destroyers, the Type 45, scheduled to enter service in 2009.

As with many of today's network-centric systems, the SDR uses the very latest technology. For example, the baseband boards in the MSN 8100-H are densely populated and use fine pitch high density connectors, as well as large and expensive BGA/FPGA devices, all of which make the boards difficult to test by traditional methods.

To overcome these debug and testing challenges, Thales has adopted the XJTAG system for use by development and production engineers at its Crawley, West Sussex (England) facility. The XJTAG system is also being used by Thales' contract manufacturing partner. Initially, the XJTAG system will be used to debug and test the baseband PCBs that form part of the MSN 8100-H SDR.

"It made sense for us to use the JTAG chain for debug and testing, as more and more devices on our boards were JTAG-enabled – and we opted for the XJTAG system as it was the best and most cost-effective solution," said Gary Delamare, Senior Engineer, Thales. "The XJTAG system is truly intuitive – it's almost a plug and play solution. We were up and running within half a day using the tutorial and development board, and

test coverage, for digital circuits, is up around the 80 percent mark already."

The XJTAG system is designed to cut the cost and shorten the development cycle of electronic products and provides a unique solution that can test JTAG as well as non-JTAG devices. XJTAG can test a high proportion of a circuit including BGA and chip scale devices, SDRAMs, Ethernet controllers, video interfaces, flash memories, FPGAs, microprocessors and many other devices. XJTAG can be used to debug and test any circuit provided it has at least one JTAG-compliant device present.

The ability to program Flash memories and other non-JTAG devices was an important factor for Thales. By using XJEase (the XJTAG system's high-level test description language for manipulating non-JTAG devices), engineers had a rapid means of programming Flash memories both at the development stage and through into production. "Unlike other JTAG tools, XJEase enables circuit developers to re-use XJEase scripts in different projects," added Gary Delamare. "This portability is really valuable and is not available with traditional programming tools which tend to be tied to one particular processor."

Thales UK's defense activities encompass optronics, air defense, sensors, communications and naval systems. The company is the UK's second largest defense contractor and has been a supplier to the MoD since the First World War. Thales employs 10,000 staff in the UK and 60,000 people in 50 countries.

opinion

Simon Holder
Hardware Design Manager
Thales

"XJTAG is a fast, extremely versatile and cost-effective tool for generating high test coverage on PCBs containing both JTAG and non-JTAG devices. The XJTAG system has enabled us to cut the development time for debugging and testing boards by around 20 percent and it has provided the basis for a common design for test strategy, spanning development, first article build, production and field service. We looked at other boundary scan solutions but we opted for XJTAG due to its price and ease of use, and the fact that test scripts are device rather than board-centric, which makes them reusable on different projects."

THALES

Company	Thales
Nature of business	UK's second largest defense contractor
Main product	Flight simulation, secure transactions, integrated communications, naval and air defense systems
Customers	Military and industrial
Locations	60 sites across the UK
Employees	10,000 in the UK, 60,000 worldwide
Revenues	£1.1bn in 2004
Web site	www.thalesgroup.com

QSI Corporation

QSI Corporation Deploys XJTAG® Through Development, Production and Service

In activities spanning board development, contract assembly, and after-sales service, XJTAG boundary scan is enabling QSI Corporation, the American developer of rugged embedded systems, to shorten time-consuming test tasks and pinpoint hard-to-find faults such as bad vias in multi-layer boards – and deliver powerful capabilities without requiring expensive add-ons.

QSI Corporation, located in Salt Lake City, Utah, USA, designs and manufactures rugged Human Machine Interface (HMI) modules and Mobile Data Terminals (MDT) for industrial OEMs and commercial vehicle systems integrators. The company's products include character and graphic terminals tested to comply with standards such as NEMA, IP, MIL-STD, CE, and UL. The terminals withstand high levels of shock, vibration, humidity, and other environmental conditions. They are programmable, customizable, and feature many configurable hardware options to match customers' exact needs.

The boards for QSI's HMI and MDT products are assembled by a manufacturing partner, which tests the finished boards using fixtures provided by QSI. However, if a defect prevents the core logic from operating, the fixture cannot be used. QSI has overcome this challenge by incorporating the XJTAG boundary scan system into the test equipment provided. The run-time-only XJTAG variant, XJRunner, makes this a cost-effective option. QSI is also using XJTAG in their own technical departments, including engineering and product servicing.

Because the company's products are subjected to rigorous usage in the field, QSI aims to provide responsive service and repair facilities for their customers. Using conventional test techniques to diagnose faults in returned units, service engineers could expect to spend more than one hour per board to probe all of the data, address and control lines. "Using XJTAG in our service department has taken a one- to two-hour task and solved it in 15 minutes," explains Eric Anderson, Electrical Test Engineer at QSI.

According to Anderson, two of the most powerful aspects of XJTAG that have enabled this dramatic speed up are the XJEase high-level scripting language and the graphical environment that helps users set up projects and visualize the circuit under test. "The scripting language is a very powerful feature that allows us to test almost any device connected to the processor. We are using it to test components from LEDs to ROMs," Anderson continues. "Moreover, we can test devices supporting interfaces such as I²C and SPI without having to buy expensive add-ons, which some other systems require. XJTAG provides online libraries that allow us to test these devices at no extra cost."

Describing XJTAG's graphical application, XJAnalyser, Anderson highlights the control it provides as being central to reducing test and debugging time. "XJAnalyser gives us complete control of most of the pins of a processor," he says. "We are able to toggle individual pins, which has helped trace obscure faults like bad vias in minutes rather than hours."

The QSI engineering group is also using XJTAG to bring up new designs. The company's latest board has two JTAG devices, and Anderson says the engineering team has used XJTAG to program and test one of the devices, and then to test the remainder of the product. "There is so much freedom in XJTAG that other testers do not provide. As engineers, we want to be able to control every part and see exactly what is happening at any place in the system. XJTAG gives us that freedom," he concludes.

opinion

Eric Anderson
Electrical Test Engineer
QSI Corporation

"XJTAG has taken a one- to two-hour task and solved it in 15 minutes. The XJEase scripting language is a very powerful feature that allows us to test almost any device connected to the processor. We can test devices from LEDs to ROMs, and can also test I²C and SPI devices without having to buy expensive add-ons."

"We can also toggle individual pins to trace obscure faults within minutes. As engineers, we want to be able to control every part and see exactly what is happening at any place in the system. XJTAG gives us that freedom."

QSI CORPORATION

Company	QSI Corporation HQ USA
Nature of business	Design and manufacture operator interface terminals for industrial, commercial and vehicle applications
Main products	Rugged, configurable human machine interface (HMI) and mobile data terminal (MDT) products
Customers	Industrial OEMs and commercial vehicle systems integrators
Location	Salt Lake City, USA
Incorporated	1983
Web site	www.qsicorp.com

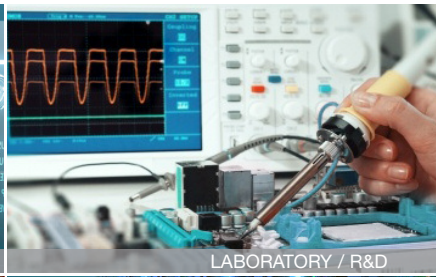
Finisar

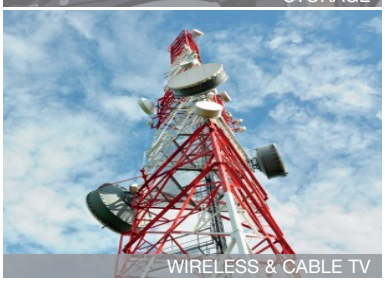
www.xjtag.com


STORAGE

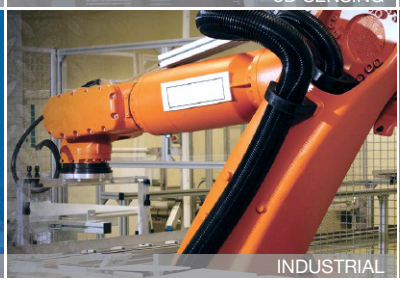

MILITARY & AEROSPACE

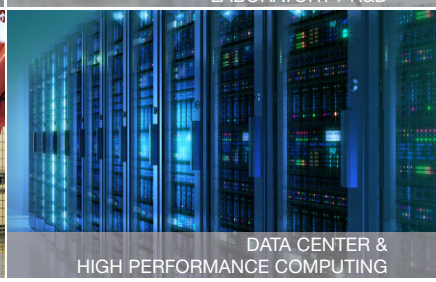

3D SENSING


LABORATORY / R&D


WIRELESS & CABLE TV


ENTERPRISE, ACCESS & TRANSPORT


INDUSTRIAL


DATA CENTER &
HIGH PERFORMANCE COMPUTING

XJTAG® Boundary Scan Delivers Beyond Expectations for Optical Communications Leader

"Finisar, which produces high-performance optical communication linecards, initially invested in XJTAG boundary scan to overcome a particular test challenge. In practice, XJTAG's ease of use and powerful features provided much greater scope to increase coverage and streamline testing to ensure only perfect boards leave the factory."

Finisar, a global optical communications technology leader, is responsible for designing equipment such as reconfigurable optical add-drop multiplexer (ROADM) linecards based on Wavelength Selective Switching (WSS) technology. ROADMs boost efficiency and flexibility in metro optical networks by switching data traffic at the wavelength layer. The boards are high-value items built around a microprocessor system embedded in an FPGA.

The boards are built at Finisar's manufacturing partner Fabrinet, and are tested at various stages using boundary scan as well as as X-ray, optical inspection and in-circuit tests. "We want to identify any defects as early as possible to ensure optimum efficiency," says Finisar Test Engineer Gili Goldfarb. "We are using XJTAG boundary scan immediately after the soldering process to pinpoint defects quickly and also to program devices on the board."

Goldfarb explains that Finisar first contacted local XJTAG distributor Polaris Systems Engineering to help test connections to BGA devices, but is now taking advantage of XJTAG to test many other devices including an adjustable power supply and analogue circuitry. "We have full access to the pins of devices connected to the boundary scan chain such as the FPGA, configuration Flash and Ethernet PHY, and are able to test other chips connected to the FPGA by emulating bus signals. In this way, XJTAG gives us flexibility to read and check many analogue signals on the board."

Controlling and monitoring the pins on boundary scan devices is easy using XJTAG's circuit visualization and debugging tool, XJAnalyser. Test engineers can get low-level access to setup pin states and manipulate busses. They can also take advantage of the color-coded graphics to assess logic levels or other properties such as input/output on the screen in real time.

Finisar's Gili Goldfarb also highlights easy code development as a factor that has helped the company maximize the return on its investment in boundary scan. Creating a high-level program to generate test vectors is straightforward using XJTAG's scripting language XJEase, and permits complex tests that are not possible with other boundary scan systems. "XJEase simplifies test development, and we can easily adjust the code to suit our purposes," he adds.

The Finisar test engineering team uses the XJDeveloper development environment in-house to create a set of XJTAG tests for each design. These tests are then passed to Fabrinet to test production units using XJRunner, a specialized runtime environment. XJRunner is optimized for production, and executes pre-compiled XJDeveloper projects including testing and in-system programming.

Having initially introduced boundary scan to overcome the specific challenge presented by BGA devices, Finisar is now maximizing the return on its investment in XJTAG. "XJTAG delivers an excellent price/performance ratio and has helped us realize the potential to achieve very high test coverage. We are now reaping the rewards of using more boundary scan components and focusing on testability at an early stage of design," concludes Gili Goldfarb.

opinion

Gili Goldfarb
Test Engineer
Finisar Israel

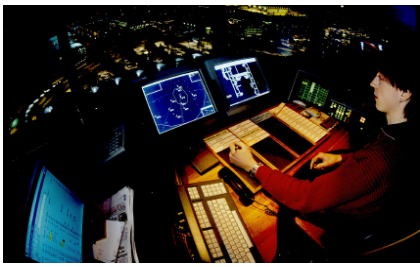
"We are using XJTAG boundary scan immediately after the soldering process to pinpoint defects quickly and also to program devices on the board. XJTAG gives us flexibility to read and check many analogue signals on the board."

"XJEase simplifies test development, and we can easily adjust the code to suit our purposes."

"XJTAG delivers an excellent price/performance ratio and has helped us realize the potential to achieve very high test coverage. We are now reaping the rewards of using more boundary scan components and focusing on testability at an early stage of design."

FINISAR®

Company	Finisar Corporation, HQ USA
Nature of business	Global technology leader in optical communications
Main products	Fiber optic subsystems and components for high-speed voice, video & data communications for telecommunications, networking, storage, wireless, and cable TV
Customers	Global datacom & telecom OEMs
Location	Azrieli Center Holon, Israel. Headquarters in the USA; R&D facilities, manufacturing sites, and sales offices worldwide.
Web site	www.finisar.com



Curtiss-Wright Selects XJTAG® to Debug and Test Complex PCBs

"Curtiss-Wright Controls Embedded Computing, a leading designer and manufacturer of commercial-off-the-shelf (COTS) systems and board level products, is using the XJTAG boundary scan development system to improve the process of debugging and testing its range of radar, video and graphics products."

Curtiss-Wright's video and graphics group designs rugged and benign solutions for customers across the defense, aerospace, commercial and industrial marketplaces. Its expertise encompasses radar pre-processing, scan conversion, tracking and display integrated with TV video, infra-red and sonar, as well as compression, decompression and distribution of radar and TV video across wide and local area networks.

The group's products and solutions are used throughout the world in vehicle, airborne and shipborne command and control consoles, vessel tracking, air traffic control and air defense systems. Customers include, among others, BAE Systems, Boeing, DRS Technologies, EDO Corporation, Lockheed Martin, Northrop Grumman and Raytheon.

Faced with the challenge of improving the process of debugging and testing its latest range of highly complex ball grid array (BGA) populated printed circuit boards, engineers at Curtiss-Wright's video and graphics group in Letchworth, England, set out to find a cost-effective boundary scan solution.

"We selected the XJTAG system due to its price, the speed and accuracy of fault diagnosis, and because the re-usable test scripts can be ported from project to project and migrate through design, prototyping to production and beyond," said Alan McCormick, Managing Director of Curtiss-Wright's Video and graphics group.

XJTAG is now being used to debug and test products such as Curtiss-Wright's Sabre imaging platform, which combines a high-performance PowerPC processor with a multi-head, multi-layer graphics video and radar display capability in a single VME slot. It is also being utilized on the Osiris dual-channel radar interface board.

"Using XJTAG, we are able to very quickly debug and test both the boundary scan and cluster devices on our Sabre and Osiris boards, many of which are inaccessible to traditional test methods such as flying probes, logic analyzers, oscilloscopes and X-ray systems," added Stuart Allen, senior hardware engineer at Curtiss-Wright's video and graphics group.

XJTAG enables engineers to test a high proportion of the circuit including BGA and chip scale packages, such as SDRAMs, Ethernet controllers, video interfaces, Flash memories, FPGAs and microprocessors. The ability to test both boundary scan and cluster devices gives engineers valuable extra flexibility to design tests for critical parts of the board.

"We are using FPGAs on many of our cards and with the XJTAG circuit visualization tool (XJAnalyser), we can read and write to all the thousands of device pins on an FPGA or another JTAG-enabled device and validate that every pin is functioning whether or not it is being utilized in the first release of the product or not," added Stuart Allen, "this capability is very valuable."

The XJTAG development system is a cost-effective solution for debugging, testing and programming electronic printed circuits boards and systems throughout the product lifecycle. The XJTAG system reduces the time and cost of board development and prototyping by allowing early test development, early design validation of CAD netlists, fast generation of highly functional tests and test re-use across circuits using the same devices.

opinion

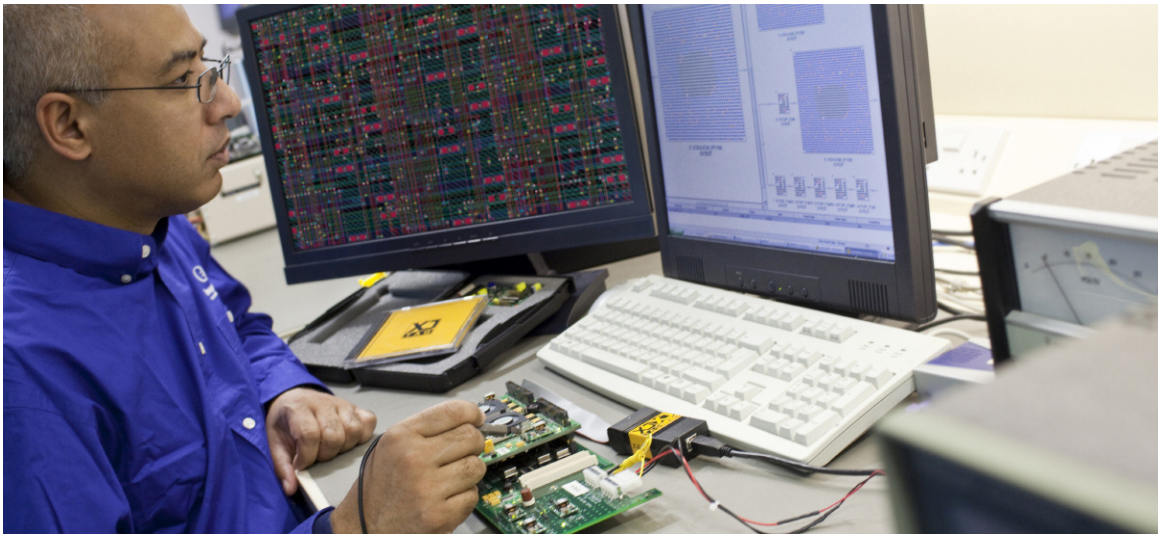
Alan McCormick
Managing Director
Curtiss-Wright
Video and graphics group

"We selected the XJTAG boundary scan development system due to its price, the speed and accuracy of fault diagnosis, and because the re-usable device-centric test scripts can be ported from project to project and migrate through design, prototyping to production and through into field test roles. Using XJTAG, we can very quickly debug and test both the boundary scan and cluster devices on our boards, many of which are inaccessible to traditional test methods such as flying probes, logic analyzers, oscilloscopes and X-ray systems."

CURTISS WRIGHT Controls Embedded Computing

Company	Curtiss-Wright Controls Embedded Computing (Video and graphics group)
Nature of business	Designer and manufacturer of rugged radar, video and graphics products
Main product	Products provide radar pre-processing, scan conversion, tracking and display integrated with TV video, infra-red and sonar
Customers	Defense, aerospace, commercial and industrial system integrators
Locations	Letchworth (UK), plus group sites in the United States, Canada and Europe
Web site	www.cwembedded.com

Imagination Technologies



Durgesh Patel, Senior Design Engineer

Mark Dunn, VP Engineering with Simon Payne, CEO XJTAG

Graham Deacon, Director of Verification

Imagination Develops SoCs Faster Using XJTAG® Boundary Scan

"Imagination Technologies, a leading IP innovator, is using XJTAG boundary scan to accelerate development of System-on-Chip designs based on industry-leading multimedia IP. Using the system to debug early test hardware, engineers are able to develop tests even before prototype boards are delivered, and to identify any manufacturing flaws within minutes before commencing design verification."

Imagination Technologies provides comprehensive System-on-Chip (SoC) design services including fully customized solutions or standardized platform implementations, based on Imagination's industry-leading IP portfolio. The IMGworks group develops complete SoC solutions using Imagination's IP cores, and works with chip companies as well as leading consumer-product brands targeting mobile- and multimedia-products markets.

"We have developed a state-of-the-art design flow, to provide a fast and low-risk path to production for our customers, says Mark Dunn, VP of Engineering at IMGworks. "Speed is vital, as our customers are typically aiming for a very short market window and rely on us to help them beat their competitors to market."

As a part of its IP development flow, Imagination builds small numbers of boards and test chips for verification purposes, and also produces development systems as necessary for specific customer contracts. The hardware is usually complex, typically having high I/O interconnect density with complex FPGAs and many signals running on internal layers that cannot be probed. "When the first prototypes come back from manufacturing, everything is new: the board, the software, the chip design," explains Graham Deacon, Director of Verification. "Obviously we want to start design verification quickly, so we need a fast way to track down any production defects."

Historically, Imagination's engineers have used socket-based testing to identify hardware faults. This has involved configuring the FPGA to carry out functional tests. Connectivity is very difficult to check in any other way, according to Deacon. In practice, however, significant resources must be committed to develop effective board-level tests by changing the function of the board. "It can involve a couple of weeks of effort," he suggests.

A faster and more efficient approach was needed, but although the team at Imagination had knowledge of various boundary scan test systems, only XJTAG offered the functions and ease of use they were looking for. "XJTAG's engineers demonstrated the system using our own assemblies, which gave us complete confidence that we could quickly produce the tests we need," says Mark Dunn.

Imagination is now using XJTAG to test and debug prototypes, test assemblies and customer development boards. Highlighting the system's convenient and powerful features such as the built-in connectivity test, Graham Deacon explains that connectivity testing and further tests using XJTAG are performed directly after the initial power check on any new board. "XJTAG has significantly reduced test-development effort, and we can compile effective test scripts even before the hardware is ready." Test execution time is usually around 10 minutes, and the tests filter out the majority of assembly flaws, whereas socket-based tests used to take over one hour to execute.

"XJTAG has much greater functionality than we expected. We can test memory interfaces and non-JTAG components well beyond the scan chain. This makes the system very flexible for debugging in the laboratory. It's a powerful engineering tool, which is perfect for our requirements," says Dunn.

opinion

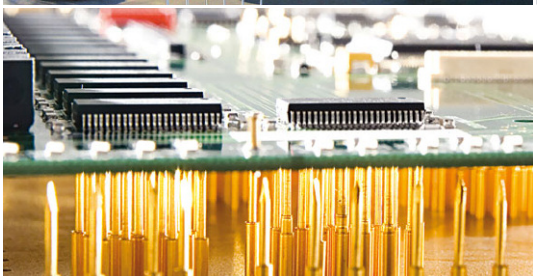
Mark Dunn
VP Engineering, IMGworks
Imagination Technologies

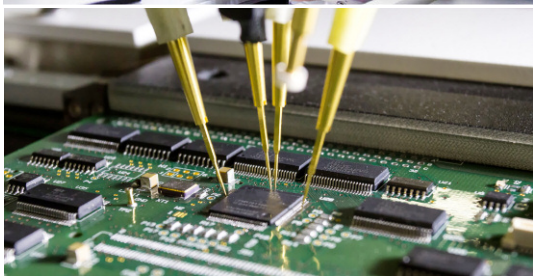
"XJTAG has significantly reduced test-development effort, and we can compile effective test scripts even before the hardware is ready. Testing with XJTAG is our first action after the initial power-up check of a new board, and we are able to test a high proportion of each board for any manufacturing defects within around ten minutes."

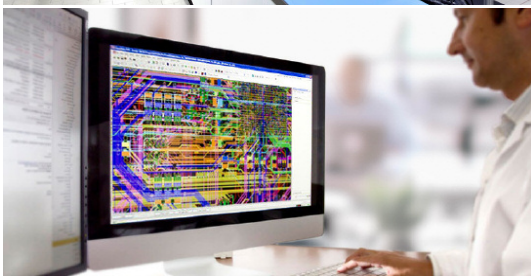
"XJTAG has much greater functionality than we expected. We can test memory interfaces and non-JTAG components well beyond the scan chain. This makes the system very flexible in a lab debug environment. It's a powerful engineering tool."

Imagination

Company	Imagination Technologies
Nature of business	Flexible and customizable IP for customer SoC applications
Main product	POWERVR, META, and ENSIGMA IP core technology families
Customers	Consumer electronics markets such as digital radio & audio, mobile phones, personal media players, navigation & driver information, mobile internet devices, digital TV & set top box, mobile TV...
Location	HQ Kings Langley, UK Offices in Far East, India, USA
Web site	www.imgtec.com



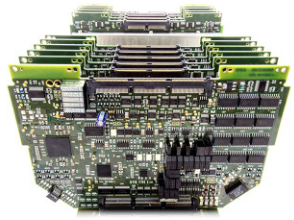




SPEA and XJTAG® Combine the Best of Flying Probe and Boundary Scan

"Test engineers face increasing pressure as board designs are becoming more densely populated with devices that have little or no access to their pins, and the space for test points is under pressure. SPEA has taken a lead in the test market, offering their clients a one stop solution by integrating boundary scan with its world renowned flying-probe and bed-of-nails testers."

SPEA is a world-leading automated test equipment (ATE) manufacturer serving the semiconductor and electronics industries, with clients in markets such as aerospace, aeronautics, telecommunications, automotive, medical, consumer and security. The company's bed-of-nails and flying probe board testers are multi-function test systems that utilize additional techniques such as optical inspection, 3D laser checking and open-pin detection to ensure maximum test coverage. SPEA customers are able to give end users the assurance of perfect board performance over many years, with minimal field returns.



Each new generation of boards increases the challenge to maintain high levels of test coverage, as PCBs become more complex and densely populated, fewer test points are provided, and new component package styles compromise the ability to probe I/O pins. To ensure continuous improvement and that testing Ball Grid Array (BGA) devices on dense boards does not impact test coverage, SPEA has introduced boundary scan testing on its bed-of-nails and flying probe testers.

Boundary scan permits testing of devices and connections on nets connected to JTAG-compatible components on the board, via a conveniently located test port. Where device I/O pins are inaccessible, or test points are not available, boundary scan enables engineers to maintain a high level of test coverage. Boundary scan is also able to generate accurate diagnostics that can pinpoint the locations of any faults that are detected.

SPEA and XJTAG engineers have worked together to ensure superior performance on the combined test platform, in order to provide best-in-class test capability and optimum value for customers.

"Boundary scan testing has several key strengths that complement SPEA's expertise in the electronics test market," explains Stefano Ghibò, Technical Sales Specialist at SPEA. "XJTAG is powerful and easy to use, which enables us to maximize the advantages of built-in boundary scan for our customers."

"To complete the integration of boundary scan and in-circuit test functionality, the SPEA team has re-optimized the overall test strategy to optimize test cycle times. The combined system also implements a test coverage report that blends the data from the different test techniques."

Stefano Ghibò describes the support provided by engineers from both companies as paramount to help clients with their projects. "Our engineers are readily available to answer customers' questions, and help them to maximize their test coverage for boards under test."

Testing times may be ahead as electronic circuits become more complicated; however, the collaboration between leading suppliers is not only helping address the challenges facing engineers today but is also creating test solutions fit for the future.

opinion

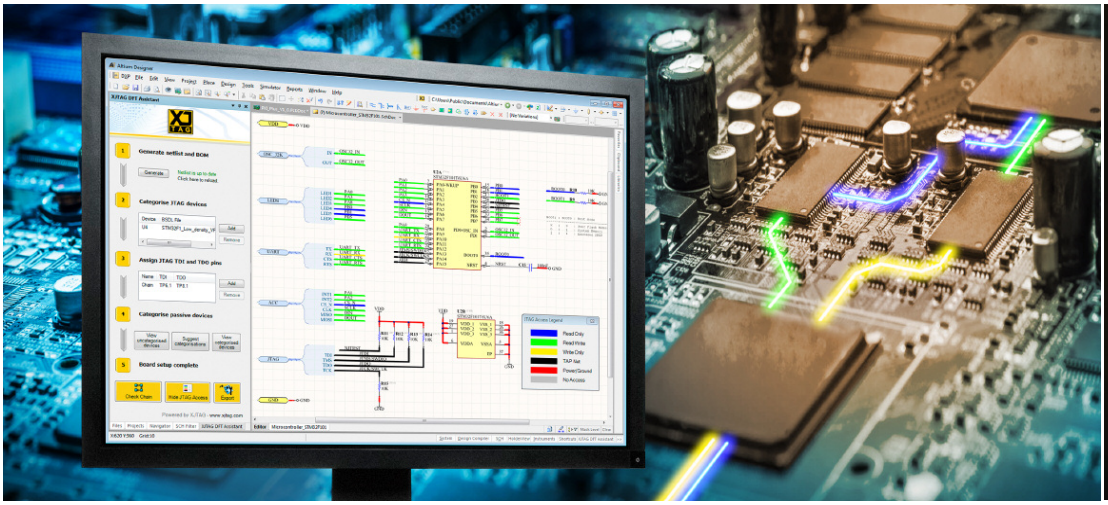
Stefano Ghibò
Technical Sales Specialist
SPEA

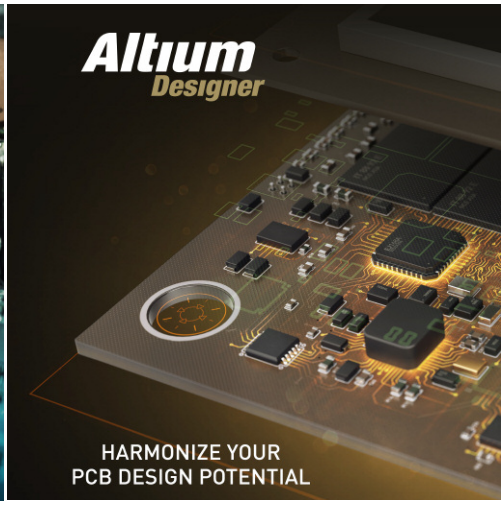
"Boundary scan testing has several key strengths that complement SPEA's expertise in the electronics test market. XJTAG is powerful and easy to use, which enables us to maximize the advantages of built-in boundary scan for our customers."

"To complete the integration of boundary scan and in-circuit test functionality, the SPEA team has re-optimized the overall test strategy to optimize test cycle times. The combined system also implements a test coverage report that blends the data from the different test techniques."

SPEA

Company	SPEA Spa HQ Italy
Nature of business	A world leading designer and manufacturer of Automatic Test Equipment (ATE) for microchips and electronic boards
Main product	Flying probe testers, bed-of-nails testers, power functional testers
Customers	Global semiconductor and electronics industries
Founded	1976
Employees	Approx. 600
Location	Volpiano, Italy. Offices worldwide.
Web site	www.spea.com





Altium Designer® Integrates XJTAG® Boundary Scan to Boost PCB Testability

"The Altium Designer PCB development environment has powerful features that help engineers manage their designs from schematic to product. Altium sought XJTAG's expertise in boundary scan to extend Altium Designer with Design-For-Test features that enable designers to find and correct errors and harness boundary scan's power to maximize testability."

Altium Designer is trusted by engineers for its rich features, which not only accelerate design capture and help overcome layout and routing challenges, but also help verify mechanical fit and coordinate the entire design-to-production process. Its wide-ranging capabilities extend beyond design entry, to include managing design assets to facilitate reuse, checking component pricing and availability, verifying design files, and supporting design with advanced technologies such as rigid-flex PCB.

"Our aim is to ensure that Altium Designer is always the industry reference, delivering high-value functionality that maximizes design efficiency and empowers users to achieve the highest possible PCB quality, manufacturability and reliability," says Daniel Fernsebner, Corporate Director, Technology Partnerships and Business Development, Altium. "Our customers look to Altium Designer to help take advantage of the latest fabrication technologies, and to provide innovative features that support accurate and intuitive design."

Altium Designer is an extensible platform that supports the addition of supplemental functionality through approved Third-Party extensions. Altium saw the customer benefits of adding boundary scan chain verification to Altium Designer and turned to the experts, XJTAG, to develop an extension that could deliver those Design-For-Test (DFT) capabilities.

"By collaborating with XJTAG, we've been able to expand the value of the Altium Designer platform for our customers with the first-ever extension to verify boundary scan chain design and ensure DFT best practices are achieved," explains Daniel Fernsebner. "The XJTAG boundary scan system provides engineers with a complete Design for Testing experience all within the unified design environment they know and trust."

The result of the successful collaboration between the two companies is XJTAG DFT Assistant for Altium Designer, which comprises two powerful features: XJTAG Chain Checker, and XJTAG Access Viewer. Together, they validate the correct implementation of boundary scan chains to allow designers to identify and correct potential problems during schematic capture, thereby avoiding costly board respins. XJTAG Chain Checker verifies the boundary scan chain is correctly routed and is in compliance with DFT best practices, reporting any connection, termination or compliance pin errors to the user. The XJTAG Access Viewer, which can be activated at any time with a single click, gives an intuitive color-coded view of the JTAG test access achievable across an entire design, on each net. All the analysis is completed without leaving the Altium Designer environment.

XJTAG DFT Assistant for Altium Designer also bridges the gap between board design and test development by exporting the information added in Altium Designer as an XJDeveloper project. XJDeveloper is the XJTAG test development environment, which is widely used to accelerate debugging of prototype hardware, and to augment traditional in-circuit and functional testing on the production line resulting in increased test coverage and faster cycle times.

Daniel Fernsebner sums up the result, "By combining XJTAG's wealth of experience in solving PCB issues and 30 years of PCB design technology from Altium, we've been able to provide the most accessible DFT solution for our customers at no cost. XJTAG DFT Assistant for Altium Designer is highly effective at helping our customers save valuable time, minimize avoidable costs, and enhance the quality of their boards."

opinion

Daniel Fernsebner
Corporate Director, Technology Partnerships and Business Development
Altium

"Our aim is to ensure that Altium Designer is always the industry reference, delivering high-value functionality that maximizes design efficiency and empowers users to achieve the highest possible PCB quality, manufacturability and reliability."

"The XJTAG boundary scan system provides engineers with a complete Design for Testing experience all within the unified design environment they know and trust."

"By combining XJTAG's wealth of experience in solving PCB issues and 30 years of PCB design technology from Altium, we've been able to provide the most accessible DFT solution for our customers at no cost. XJTAG DFT Assistant for Altium Designer is highly effective at helping our customers save time, minimize costs, and enhance the quality of their boards."

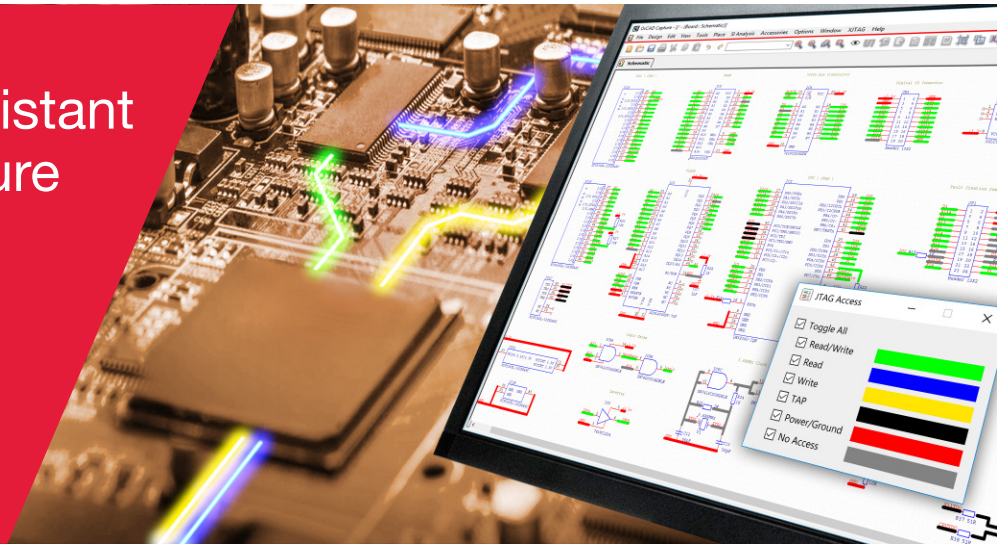
Altium

Company	Altium Limited HQ USA
Nature of business	Electronic Design Automation (EDA) for 3D PCB design and embedded system development
Main products	Altium Designer®, Altium Vault®, CircuitStudio®, PCBWorks®, CircuitMaker®, Octopart®, TASKING®
Customers	Global electronic design community
Founded	1985 in Hobart, Australia
Employees	400 worldwide
Revenues	US $76.1 million
Location	San Diego, California. Headquarters in Germany, China and Australia.
Web site	www.altium.com

New XJTAG® DFT Assistant tool for OrCAD® Capture

Free, easy-to-use 'Design for Test' plugin so you can catch errors before layout and avoid costly re-spins

FlowCAD



"Developed by XJTAG®, the software for OrCAD Capture will significantly increase the Design for Test and Debug capabilities of the schematic capture and PCB design system."

OrCAD Capture has a multitude of features that help engineers manage their PCB designs efficiently, from initial schematic entry through design analysis and rule checking, layout optimization, component selection and BOM management. Tools such as automated wiring accelerate laborious processes, viewers with color-coding help inspect nets and navigate connection hierarchies, and database and search tools help streamline component selection.

Engineers now need to be able to determine at the schematic stage how they can best implement Flash programming, JTAG debugging and boundary scan testing. With OrCAD Capture users now have access to XJTAG DFT Assistant to help check that JTAG chains on the board are setup correctly and ready to support testing, debugging and programming. By eliminating errors and helping ensure the JTAG chain is used to its full potential, DFT Assistant helps boost test coverage and ensures that prototype boards can be tested and programmed with boundary scan as soon as they are received back from assembly.

Verifying designs at the schematic stage delivers advantages from the beginning of the product lifecycle. It can help check for errors before any hardware is built. The extra effort really starts to show its value when the first prototype boards are produced enabling connection tests to be done in minutes whereas manual probing can take hours to locate shorts or opens if the board will not start up. Having a working JTAG capability early in the debug stage will enable accelerate board bring up and enable firmware programming and CPU debugging as well as boundary scan testing.

"We saw that our customers could benefit from direct integration of JTAG in OrCAD Capture," comments Kishore Karnane, Director Product Management, Cadence OrCAD Solutions. "XJTAG was the ideal partner to help us achieve this, bringing their specialist knowledge and their expertise in testability issues and design."

The result of this collaboration, XJTAG DFT Assistant for OrCAD Capture, consists of the XJTAG Chain Checker and XJTAG Access Viewer. XJTAG Chain Checker identifies common design issues such as connection errors in the JTAG chain design or incorrect termination of signals at Test Access Ports (TAPs). A single mistake in this area of the product design could prevent the chain from working, so it is vital that checks are done before the PCB is produced.

XJTAG Access Viewer helps engineers assess the testability of their design, and identify where coverage could be improved, by displaying the extent of JTAG access as an overlay on the schematic diagram. A helpful selection tool enables engineers to analyze specific areas of interest easily by displaying the test access to nets (read, write, power/ground or no access) individually or in groups by selecting them using checkboxes. The nets are color-coded by their JTAG access to aid inspection.

Kishore Karnane sums up, "XJTAG DFT Assistant enables us to deliver even greater value for our customers by providing powerful testability analysis. The deep understanding of JTAG / boundary scan and design automation, by XJTAG, has ensured a high-quality solution that enables users of OrCAD Capture to create even better products more quickly and efficiently."

Cadence products are distributed by FlowCAD in Germany, Austria, Switzerland, Poland, Czech Republic, Slovakia, Hungary, Romania, Bulgaria and South Africa. www.FlowCAD.com

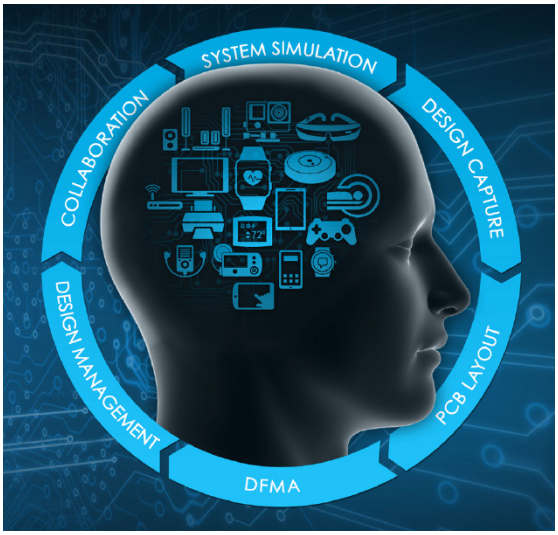
opinion

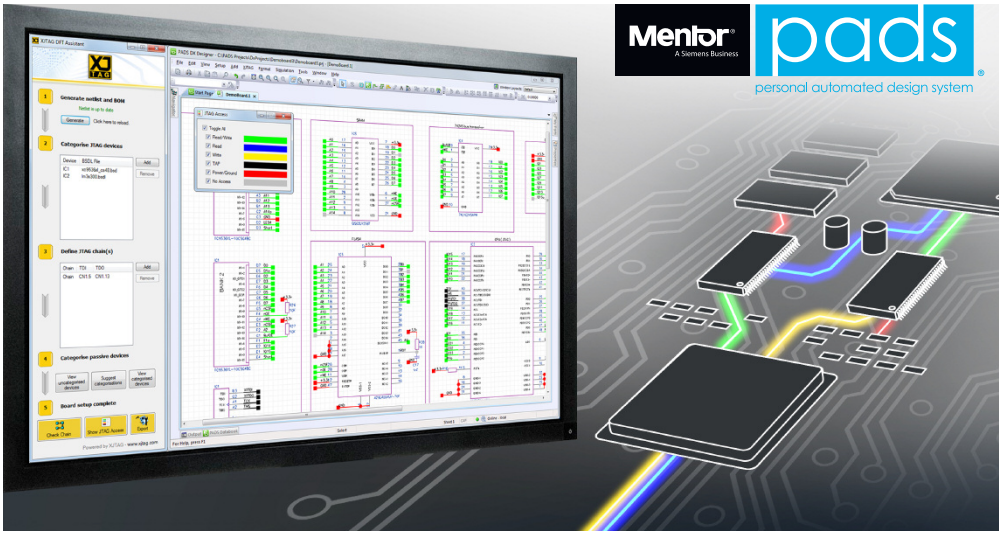
Urs Allemann
Director Design Services
Ed Electronic Design AG
Switzerland

"We need to determine early in the design phase how to maximize test coverage using the minimum number of test points. So it is vital to know what JTAG access is available at the schematic stage. The XJTAG DFT Assistant for OrCAD Capture makes it easy for us to see the test coverage as the design evolves and this allows us to optimize our testing before the PCB is produced."

cadence®

Company	Cadence Design Systems HQ USA
Nature of business	Leading provider of electronic design automation (EDA) tools, software, IP and services
Main products	Broad portfolio of tools for the design and verification of chips, packages, boards, entire systems
Customers	Global electronic design community
Founded	1988
Employees	6700+ worldwide
Revenues	US $1.7 billion
Location	San Jose, California, USA Offices worldwide
Web site	www.cadence.com





PADS® Strengthens DFT Capability with XJTAG® Boundary Scan Know-How

"Testing with Boundary can help boost test coverage, accelerate design verification and debugging, and increase production-test efficiency for Mentor, a Siemens Business. Mentor PADS users can now leverage XJTAG's experience to maximize the power of boundary scan in their designs without leaving their favorite environment, using the new, free XJTAG DFT Assistant for PADS."

Mentor PADS personal automated design solutions streamline product creation and help designers optimize all aspects of performance and manage their projects from design entry, through simulation and analysis, to sign-off for production. Optional extensions allow users to add capabilities such as advanced board layout, power-delivery analysis, thermal analysis, and support for RF design, high-speed design, and high-density or timing-critical routing.

PADS is now even more powerful with XJTAG's boundary scan test know-how built-in. "Boundary scan can add value from the beginning of the product lifecycle, and is becoming increasingly important to our customers," explains Jim Martens, Product Marketing Manager, PADS Solutions Group. "We saw the opportunity to enhance PADS with class-leading design for boundary scan test capability, by integrating the features of XJTAG's highly regarded DFT Assistant."

Boundary scan can check a high proportion of a board's connections early in the design phase, before any hardware is produced, and only requires the Test Access Port (TAP) pins of JTAG-compliant components to be correctly linked and routed to a connector. The simple four-signal interface allows easy software-based access to I/O pins that are otherwise hard to reach with probes, such as BGA I/O connections. The TAP, and traces comprising the scan chain that links the JTAG pins, occupy minimal real estate on the board.

When designing and prototyping boards, boundary scan tools help check for design errors before any hardware is built. First prototypes can be tested quickly to pinpoint connection errors, potentially saving hours buzzing out boards looking for shorts or opens that may cause errors or prevent the board starting up. In production, boundary scan can quickly check a high percentage of connections to help isolate defective boards and boost overall test efficiency.

Engineers can maximize the test coverage achievable with boundary scan by connecting JTAG compatible components into a JTAG chain. Using the JTAG chain, testing can be further extended to non JTAG compatible devices. PADS users can take advantage of XJTAG's Design-for-Test (DFT) know-how, acquired through years working with clients and refining the XJTAG test development suite, by using the XJTAG DFT Assistant for PADS now included in their favorite design environment.

XJTAG DFT Assistant for PADS features an Access Viewer that gives a graphical view of JTAG chain access across the board, which help users visualize the extent of test coverage and see how their design changes affect testability as the project progresses. In addition, the Chain Checker verifies that all the JTAG and TAP pins are correctly connected and terminated before committing to hardware. The information can be exported directly to the XJTAG test-development environment, where the testing to be carried out can be configured.

"Our customers can now use PADS to produce even better board designs that benefit from higher test coverage, faster debugging and prototyping, and more efficient testing in production. Working with XJTAG enabled us to achieve a high-quality result within a fast turnaround time," concludes Jim Martens.

opinion

Jim Martens
Product Marketing Manager
PADS Solutions Group

"Our customers can now use PADS to produce even better board designs that benefit from higher test coverage, faster debugging and prototyping, and more efficient testing in production. Working with XJTAG enabled us to achieve a high-quality result within a fast turnaround time."

"Boundary scan can add value from the beginning of the product lifecycle, and is becoming increasingly important to our customers. We saw the opportunity to enhance PADS with class-leading design for boundary scan test, by integrating the features of XJTAG's highly regarded DFT Assistant."

Mentor®
A Siemens Business

Company	Mentor Graphics Corporation A Siemens Business
Nature of business	World leader in electronic hardware and software design solutions providing products, consulting services, and award-winning support for the world's most successful electronic, semiconductor, and systems companies
Location	Corporate headquarters are located at 8005 S.W. Boeckman Road, Wilsonville, Oregon 97070-7777
Web site	www.mentor.com

XJDeveloper

Overview

XJDeveloper lets you quickly set up and run JTAG tests and programming routines. An automatically generated connection test combined with tests for non-JTAG devices, such as RAM, will check boards for short-circuit and open-circuit faults. Flash memory and EEPROMs can be programmed as well as JTAG devices such as CPLDs, FPGAs and even the internal flash in processors that have a JTAG debug interface.

Even before you have your hardware, XJDeveloper's test coverage report allows you to easily review how much of the board will be tested.

Key Benefits

- Reduce time spent debugging boards
- Improve your time to market and reduce project risk by early design verification
- Reduce your test development time by reusing tests from prototype/design in manufacturing and field support
- Ongoing time savings by test reuse across projects

Rapid test development

XJDeveloper can help you speed up test development by making suggestions about how to categorise the devices and nets in the circuit. If you have BOM information, it will also suggest which model from the installed libraries should be used for each device.

The libraries contain models for simple passive devices such as resistors, complex ICs such as DDR4 memory and devices that can be described using a truth-table such as buffers and logic gates.

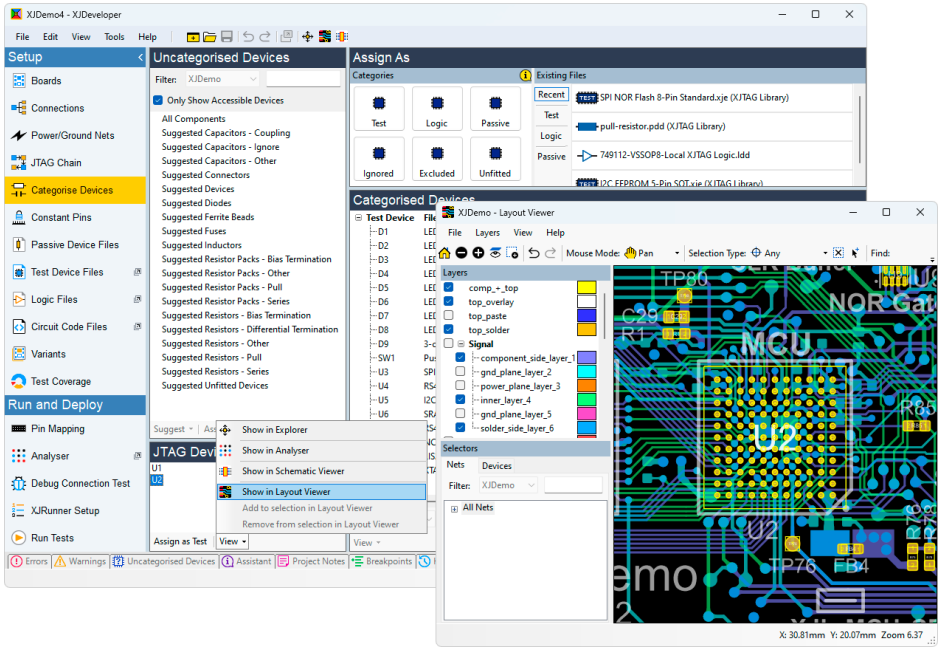
Using these models, a fully functioning test system can be created with no extra programming.

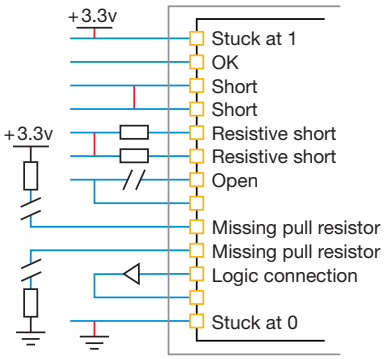
Connection test

XJDeveloper has a built-in connection test for all of the boundary scan enabled pins on your JTAG devices. It checks for a range of short-circuit and open-circuit faults, including shorts to power and ground, resistive shorts and inverted shorts. Pull-up and pull-down resistors are also verified.

As part of its functionality, the connection test also dynamically tests both data and control signals on logic devices such as buffers and logic gates.

When a fault is detected the connection test generates further targeted tests to investigate and pinpoint the location of the error.





Find a wide range of faults using XJDeveloper's connection test

Testing non-JTAG devices

XJDeveloper makes it easy to use devices in your JTAG chain to check the connections to non-JTAG devices. For example, by writing test values to a memory chip and reading them back, you can verify that the data and address lines are free from faults—without booting the processor. Advanced tests, such as sending and receiving Ethernet packets can even test parts of the board with no JTAG access.

Standard data import

XJDeveloper uses netlist information and Boundary Scan Description Language (BSDL) files to understand the JTAG devices and the connections around them. 100+ netlist formats are currently supported. One format, ODB++, also provides layout information that can be used to show the physical location of faults.

XJDeveloper

Powerful testing language

XJDeveloper's high-level programming language, XJEase, provides you with all of the functionality, flexibility and control you require to test the non-JTAG devices in your circuit.

The installed XJEase library contains tests for tens of thousands of devices. You can easily adapt them or write new tests if required, even if you don't have much software experience.

Tests are written in terms of the device being tested so you just need to describe which pins on the non-JTAG device should be driven and which ones should be read. XJEase will work out which part of the JTAG chain needs to be controlled and monitored to implement your requirements.

This not only makes it quicker to develop the tests but also allows you to reuse them for any instance of that type of device in any circuit.

By using high-level language features such as variables, loops, conditional execution, function calls, etc. you can interact with your board in real time, not just "set and check" values.

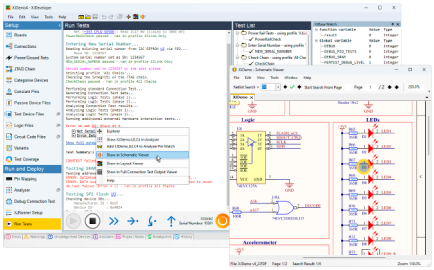
The XJEase debugger features a variable watch window and breakpoints to help get your tests running as quickly as possible.

Integrated Environment

XJDeveloper contains a fully featured debugger, allowing you to step through tests, pause at breakpoints and capture traces of the test while it's running.

The built-in Layout and Schematic Viewers allow you to quickly find any component or net in your circuit, useful when developing your tests or trying to pinpoint a fault. When you have an XJAnalyser license, that is also available inside XJDeveloper.

Once the tests are complete, they can be exported to XJRunner for production.



See the XJRunner, Layout & Schematic Viewer, and XJAnalyser datasheets for more details.

Test coverage analysis

As soon as you have a netlist and schematic, you can create an XJDeveloper project and check the level of test coverage; this is automatically calculated by combining coverage achieved through the connection test and the XJEase testing of non-JTAG devices.

You can download XJTAG's Design For Test (DFT) reference guide that covers many of the issues involved in realising the full potential of boundary scan testing.

Programming flash memory and JTAG devices

The flash memory files in the XJEase library include all of the functionality required to program the flash with an image.

To program many JTAG devices, such as CPLDs and FPGAs, XJDeveloper allows you to run STAPL / JAM or SVF files generated from the device manufacturer's tools.

The internal flash in some processors can also be programmed through the JTAG debug interface.

If your licence includes XJFlash, you can create projects in XJDeveloper which will allow accelerated flash programming, often allowing the process to run at the maximum programming speed of the flash memory, giving further time savings during board production.

Features

- Built-in adaptive connection test
- Automatic logic support
- Library of tens of thousands of standard parts
- Reuse any tests that you write
- Revisions system to handle modified versions of circuits
- Variants to allow multiple build variations on a single PCB design
- Optimises operation of JTAG chains for best performance
- Device programming
  — e.g. CPLDs, FPGAs, flash, processors
- Test coverage analysis before you go to PCB layout
- Integrated Layout & Schematic Viewers
- Advanced testing
  — e.g. Ethernet loopback
- Integration with standard test executives or custom applications
- 100+ netlist formats supported, including ODB++, RINF, Protel, PADS-PCB and ALLEGRO
- Ability to test boards with no netlist
  — just use BSDL files
- Tests 1149.1 and 1149.6 devices

Integration

XJDeveloper tests can be integrated into NI LabVIEW™, Test Stand and ATEasy using the installed examples. Bespoke test executives can also be developed in Python as well as in C#® and Visual Basic® using the .NET interface.

Test development

If all your engineers are busy, XJTAG also offers a consultancy service to create XJDeveloper test systems or bespoke device files to your exact requirements.

XJAnalyser

Overview

XJAnalyser is a visual analysis and debugging tool for devices in your JTAG chain. It provides instant chain verification as part of the simple setup wizard, and then gives you an interactive graphical view of the pins on your JTAG devices, including a waveform view of their logical values.

You can group pins into busses for easier control, and quickly generate toggling signals to trace connections around your board—useful when verifying shorts or opens. XJAnalyser also supports the STAPL/JAM and SVF standards for programming JTAG devices in-system.

Key Benefits

- Allows you to increase yields — by setting pin values and tracing signals you can quickly debug your boards, even under BGAs
- Speed up product development by allowing engineers to debug prototype and development boards in minutes rather than days
- Free up engineering resource by eliminating the need to write functional test software to check fundamental hardware connectivity

Graphical circuit debugging

When tracing a net around your board with an oscilloscope, set a pin on the net to toggle and capture the signal at different points. If you slip to another pin, you will instantly know that you are no longer tracing the signal of interest.

Quickly locate signals you are sending to a device. By monitoring pins with changing values you can, for instance, press a button and quickly locate and display the pin/ball it is connected to, even if there are many thousands of pins/balls on the devices in your chain.

See the section of the chain of interest. For devices with large numbers of pins/balls, the information can become overwhelming. XJAnalyser solves this problem by enabling you to zoom in on just the balls or pins that you are interested in. You can also display multiple views of the JTAG chain, showing different areas of interest.

Flexible control

Control the devices in your JTAG chain the way you want to. XJAnalyser offers three methods for controlling pins: directly through the graphic display, or by using the pin list or pin watch. The pin watch also allows you to group pins into busses; you can then write a value to a complete bus all at once.

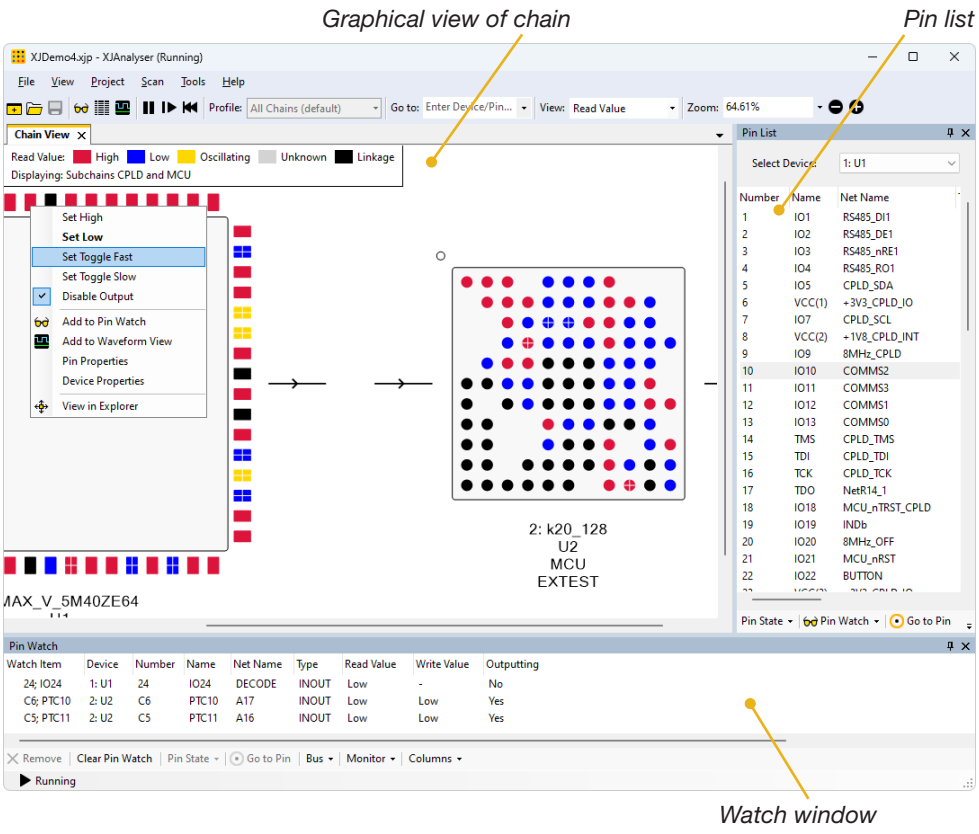
JTAG chain interaction

The intuitive graphical interface allows rapid interaction with the devices in the JTAG chain without programming or booting any devices on your board.

Monitor the states of all the I/O pins in real-time and graphically set pins to output high, low or toggle as required.

Simplify low-level access to any devices connected to a JTAG device by grouping pins together into buses (e.g. “Data” or “Address”) and setting values using convenient units (Hex, Binary, Decimal).

Avoid damaging your board — XJAnalyser generates a warning if you attempt to drive any pin to a state that would put it in conflict with a value being driven to that net from a different source.



XJAnalyser

CPLD programming

You can run STAPL /JAM and SVF files within XJAnalyser. These files are typically used to program devices such as CPLDs and FPGAs. Even if these files were created for a JTAG chain containing just a single device, XJAnalyser can run them on chains containing more devices.

Waveform Viewer

The Waveform Viewer captures and displays the digital signal levels and transitions of JTAG chain data.

It supports triggering, allowing circuit behaviour to be captured under specified conditions, such as when particularly events occur. This can greatly improve an engineering team's ability to capture key information and track down intermittent faults.

Golden board comparison

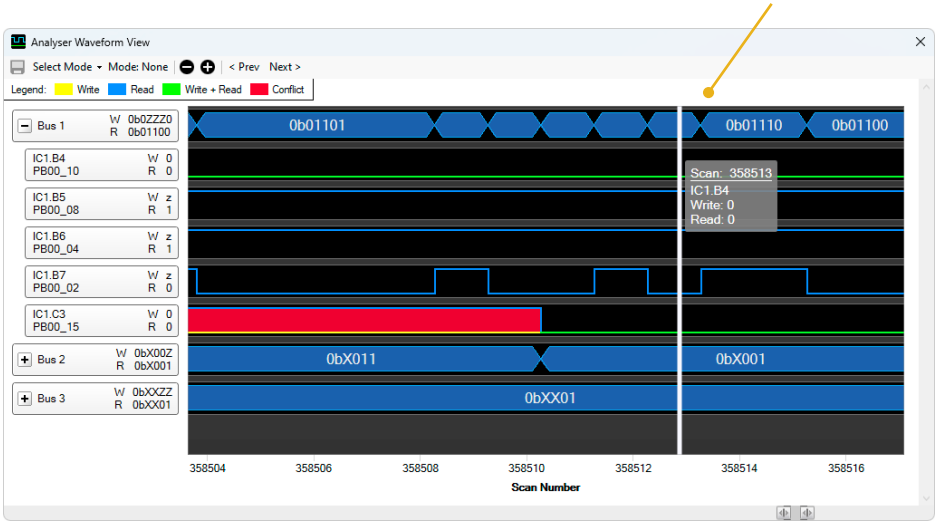
You can capture the values being driven onto the JTAG devices of a known good working board. These values can then be used to identify differences between boards exhibiting unexpected behaviour and a known good board.

Fast, simple setup

XJAnalyser has a simple setup wizard to let you start testing and debugging your board straight away. All you have to do is select a JTAG header and a library containing appropriate BSDL files and you can start working.

Even if you don't have a BSDL file, XJAnalyser will still work with the other devices.

Live waveform data view



opinion

Alistair Massarella
CEO
CRFS

"XJTAG is an absolute necessity for any company designing complex circuits that feature high pin count BGA or chip scale devices."

"XJTAG is easy to use and incredibly fast, which has enabled us to shave weeks off the development schedule for our RFeye module thereby freeing our development team from time-consuming debugging tasks."

"Test coverage is very high – we can get to over 80% of devices on the RFeye boards via the JTAG chain."

Features

- Able to test BGAs and fine-pitch devices
- Only BSDL files required to get the board up and running
- Set up pin states — e.g. low, high, toggling
- Trace shorts, opens and other signals
- Easy low-level access to device pins/busses
- Clear display of the pins/balls with variable zoom levels and split screen
- View JTAG chain data as waveforms
- Quickly find and monitor changing pins
- Program devices with SVF and STAPL files
- Plug and play
- Real-time interaction

XJTAG gives you more…

XJAnalyser also includes all of the following:

- JTAG controller — required to connect your PC to the circuit under test, available with a range of connectivity options
- Flexible licensing options so you can install the software on any number of PCs
- Demonstration hardware with full tutorial
- Support and upgrades for one year

Distributor / Technology Partner

XJRunner

Overview

XJRunner is the specialist run-time environment for executing packaged XJDeveloper projects. With a range of special features it is particularly aimed at board manufacturers.

In one package, you have connection testing, non-JTAG device testing, in-system programming, serial number handling and configurable log files for your audit trail.

Simple, secure & audited production testing

Package your XJDeveloper test system, created by design or test engineers, into a single compressed and encrypted file to ensure consistency in your testing process.

Excellent for the shop floor. A simple Run/Stop, Pass/Fail interface makes first pass testing a simple point-and-click operation. Configurable run-time messages can tell the tester about any required procedures both before and after testing each board.

Using multiple XJLinks or the 4-port XJQuad you can save time by testing a batch of boards simultaneously as a group. Alternatively, run through them independently and continuously by unplugging one board that has finished and plugging in a new one whilst tests are still running on your other XJLinks.

Each user can have a separate login. This not only identifies users for audit use, but also allows you to restrict their access to features they have been trained to use.

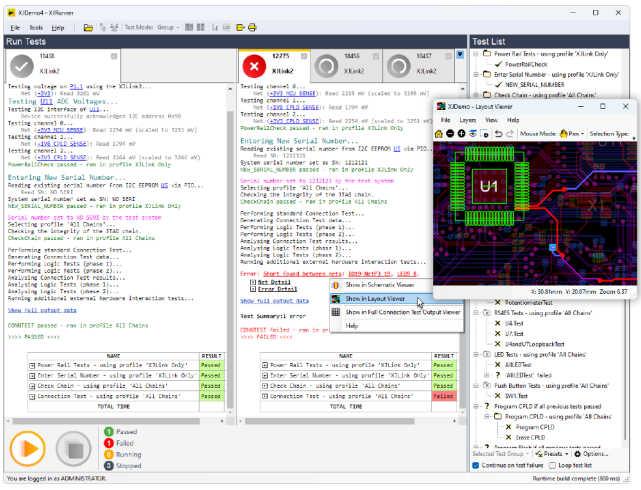
Serial numbering

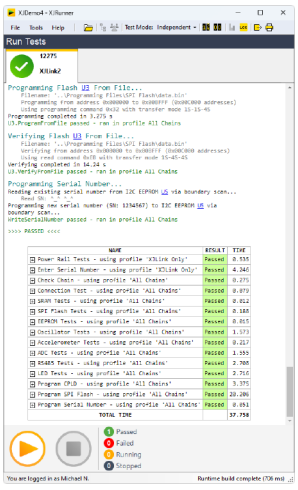
XJRunner can record serial numbers and other forms of identification such as MAC addresses or program them if required. These can be extracted from the board under test, or be input automatically or entered by the user (e.g. from a barcode reader).

Powerful, flexible testing

After a faulty board has been identified on the production line with a default set of Pass/Fail tests, advanced users can then pinpoint faults by running additional tests and debug procedures. They can also choose to run a particular test, or set of tests, a number of times, or even run a test continuously to help diagnose particularly tricky or intermittent problems on a board.

XJRunner also provides statistics on the percentage of boards that have passed/failed as well as Fault Trend Analysis, highlighting tests prone to failure.





Key Benefits

- Improves your QA through configurable logging
- Allows you to retain the power of control on how boards are tested by third parties
- User-friendly environment reduces your training costs for production operatives
- Ability to test multiple boards, simultaneously, by using multiple XJLinks

Features

- Run-time environment for XJEase tests
- Simple, controlled test execution
- Flexible serial number handling capabilities
- Log files for audit trail
- Variable levels of access for different user roles
- End user access restrictions specified at development time
- Fault Dictionary to capture the expertise of your engineers
- Integration with industry standard test executives
- Clickable links to the Schematic Viewer and Layout Viewer help you understand or locate faults on a board

XJTAG gives you more…

All of the features above are included when you buy XJRunner. The price you pay also includes:

- JTAG controller — required to connect your PC to the circuit under test, available with a range of connectivity options
- Flexible licensing options so you can install the software on any number of PCs
- Full tutorial

Distributor / Technology Partner

XJInvestigator

Overview

XJInvestigator allows you to diagnose manufacturing problems. Combining the test capabilities of XJRunner and XJAnalyser with additional diagnostic functionality, XJInvestigator is the boundary scan tool to use at your repair or rework station.

Simple, powerful and flexible diagnostic testing

XJInvestigator extracts all the information required to test and debug your boards from the same encrypted XJPack file that is used by XJRunner. To ensure consistency in the testing process the predefined test functions cannot be modified however XJInvestigator offers the extra flexibility and configuration options needed to help you to track down faults.

When a problem has been identified with a board you can select individual tests, sets of tests or additional functions not included in production testing to run. The tests can also be run continuously to help diagnose particularly tricky or intermittent problems.

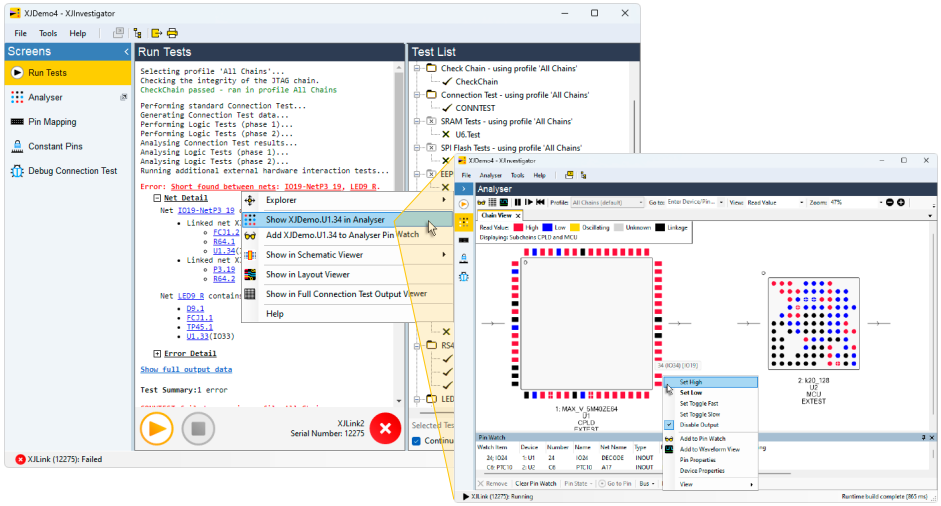
Layout & Schematic Viewers

By showing both the physical and logical organisation of a board, the Layout Viewer and Schematic Viewer* can be used to help understand and locate faults.

* The viewers are only available if you opt to include the required information in the XJPack file.

Direct control of JTAG devices

Simple ad-hoc tests can be implemented very quickly by using the JTAG-enabled devices on your board to control and monitor signals, even on BGAs. On the Analyser screen, pin values can be driven high or low or to be set to toggle simply by clicking on the pins in the graphic. The values of pins read from the board are shown in a simple colour-coded display.



Find problems with your JTAG Chain

If the production line tests cannot be run on a board due to problems with the JTAG chain then the built in Chain Debugger helps you quickly identify and fix faults so that the board can be re-tested.

Flexible interface

By keeping the test results visible while you are using Analyser and the other debugging features such as the Layout and Schematic viewers, XJInvestigator's user interface helps further streamline and simplify the debugging process.

Key Benefits

- Increase production yields – repair boards that would otherwise become waste
- Reduce board debug time – work from a single integrated environment
- Retain control on how boards are tested
- Reduce training costs – intuitive, user-friendly interface.

Features

- Repair-focused environment for XJDeveloper / XJRunner tests
- Full Connection test
- RAM, flash and other non-JTAG device tests
- Flash, FPGA, CPLD and EEPROM programming
- Layout Viewer* to show the physical location of faulty nets, pins and components.
- Schematic Viewer* to show the circuit design around faults
- Direct control of the pins/balls of JTAG devices
- Trace signals to identify shorts, opens and other faults

Pin Watch

You can put pins into a watch window allowing you to easily establish the relationships between them, even when they are from different JTAG devices. You can also build groups of pins into busses and then write values to the busses and monitor their values for more efficient testing.

Distributor / Technology Partner

XJTAG Layout Viewer

Overview

The Layout Viewer allows you to quickly find the physical location of components, nets and pins on a board. It provides the capability to view layout design data extracted from ODB++ jobs in XJDeveloper, XJInvestigator and XJRunner.

You can use the Layout Viewer to visualise any faults that are found when running tests. The Connection Test output includes clickable links to directly display all of the relevant circuit elements.

Free with XJDeveloper, XJInvestigator and XJRunner

The Layout Viewer is integrated into XJDeveloper, XJInvestigator and XJRunner to help engineers quickly identify faults.

Visualise circuit elements

The advanced graphical display highlights the physical location of selected components and nets. Individual layers can be turned on or off as required to make it easy to see specific circuit elements.

Key Benefit

Improve productivity by visualising the exact location of faults to be repaired

Features

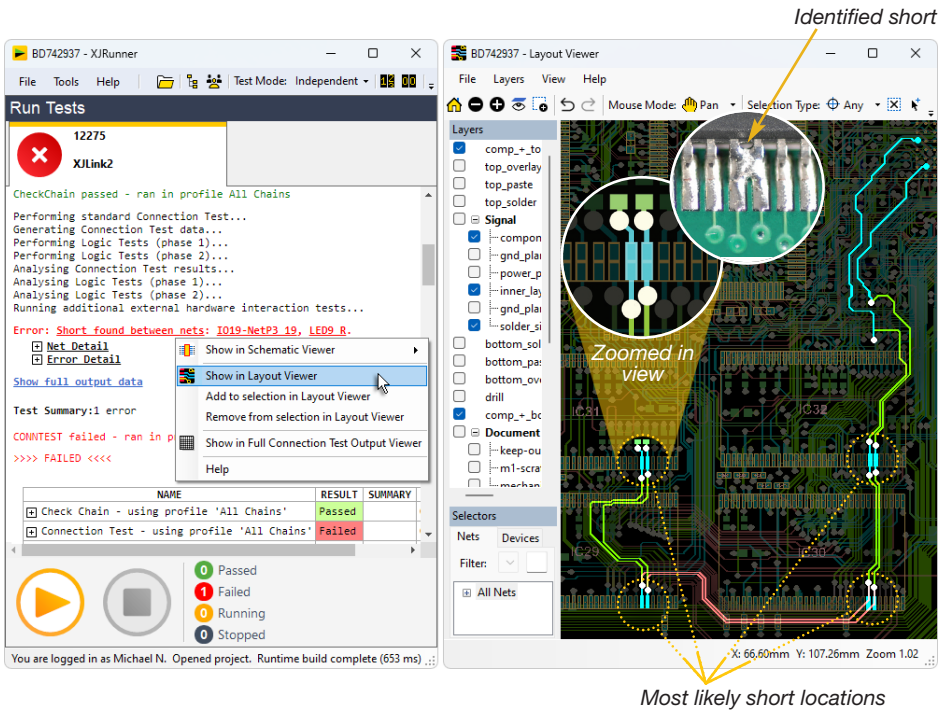
- Aids identifying likely points of failure
- Measures distance between objects
- Control over which layers are visible
- Advanced layer and zoom controls
- Exports graphics to the clipboard, a file or printer
- Import pictures for clearer display

Determine the location of faults within seconds

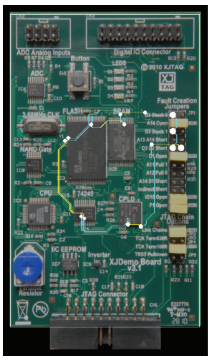
The Layout Viewer can be used to quickly locate where faults are on the board under test. As well as providing details about types of faults and the nets involved, test output can also include clickable links that allow each fault to be easily visualised in the Layout Viewer. Showing the routing of nets helps to locate the fault on the physical board, highlighting potential problem areas.

In the example below, the connection test identified two nets that are shorted together. The layout shows that it is unlikely that the fault is under the BGA device as the pins are not next to each other.

By examining the highlighted pins on the four memory devices, it was quickly identified that the problem was a soldering fault on IC31.



Import board pictures



For even more help in identifying where on a board the faults are located, pictures of the front and the back of the board can be imported. These images can then be displayed behind the CAD data with its highlighted components and nets.

Test coverage view

The test coverage of your XJTAG project can be shown on the layout view using XJDeveloper. This allows you to easily identify any areas of the board where coverage needs to be improved.

See net values live

XJTAG can display the current values of nets and pins directly on the layout view, from the Analyser screen in XJDeveloper and XJInvestigator. As net values change the display is updated automatically.

XJTAG Schematic Viewer

Overview

The Schematic Viewer allows you to quickly see the logical arrangement of circuit elements from within XJTAG. It is integrated into XJDeveloper and XJRunner and can be launched from any device, net or pin in XJDeveloper or from links embedded in the XJRunner test output. This saves having to continually change applications to view the schematic.

You can use the viewer to quickly understand how a device is being used in a circuit, to help identify faults and debug tests. Simple links take you straight from your XJTAG system and highlight the relevant section of the schematic in the viewer, while the intelligent netlist search allows you to navigate directly to other elements of the circuit.

Key Benefits

- Speed up test creation and debugging of prototype and manufactured boards
- Improved search functionality*

Features

- Integrated in XJDeveloper and XJRunner
- Shows best match first when searching for pins/nets/devices
- Intelligent, learning search
- Searches meta data as well as surface text in PDF documents*

*Requires searchable PDF documents

Included free with XJDeveloper and XJRunner

The Schematic Viewer is integrated as a standard feature of XJDeveloper and XJRunner to help engineers quickly understand the function of the circuit.

Safe and secure

For manufacturers to use the viewer in XJRunner, you have to explicitly export the schematic information from XJDeveloper. Conversely, if your schematics need to be kept confidential, do not export them to XJRunner.

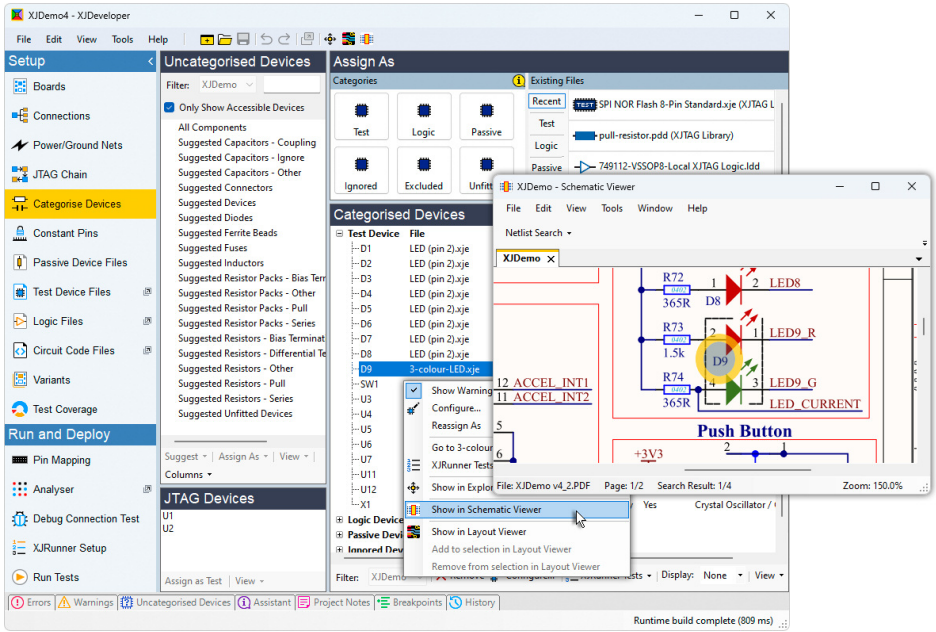
Find the right device, net or pin in seconds

Whether you are developing tests or debugging boards, searching for a device, net or pin on a schematic is a common task. The Schematic Viewer simplifies this process using its smart textual analysis as well as PDF bookmarks to take you to the most relevant section of the schematic.

The viewer is very helpful when setting up your XJTAG test system as you can use simple context menus to view the section of the schematic related to any device. These menus are available throughout the system and can be used at every stage of the setup, even when reviewing the test coverage that XJTAG reports in its Design For Test analysis.

Once you receive your first prototype hardware and start running tests, the Schematic Viewer saves you time and effort by allowing you to navigate directly to those nets identified as faulty. This can help you understand whether any problems are caused by real hardware faults or are simply configuration issues – such as unfitted components.

If you need to check if a device has been correctly fitted to your board you can use the XJTAG Layout Viewer to pinpoint its physical location.



Generic data import

The viewer can be used with the output from any schematic capture tool that can produce standard PDF documents.

Distributor / Technology Partner

XJFlash

Overview

XJFlash is an advanced and innovative method for In-System Programming (ISP) of flash devices through JTAG. Using XJFlash you can achieve flash programming speeds up to 50 times faster than those possible using conventional boundary scan techniques.

Custom Solutions – Automatically Generated

XJFlash allows you to automatically generate customised programming solutions for the flash devices connected to FPGAs on your board.

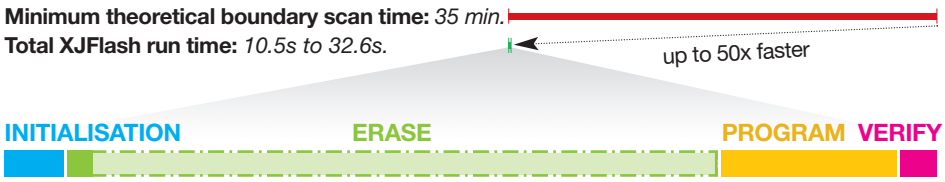
The functional capabilities of the FPGA are harnessed to provide the fastest possible programming speeds. XJFlash automatically generates a custom design for each FPGA/flash combination, allowing you to achieve the best programming times, whilst not requiring you to do any FPGA development.*

Whether you are using SPI, QSPI or parallel NOR flash connected to an FPGA from Altera, Xilinx, Microsemi or Lattice – XJFlash will provide you with a programming solution optimised for your board.

**A licensed version of the relevant FPGA manufacturer's tools will be required during the configuration of XJFlash. Free versions are sufficient for many devices.*

XJFlash Example Timings

Minimum theoretical boundary scan time: *35 min.*
Total XJFlash run time: *10.5s to 32.6s.*



XJFlash will automatically step through four stages each time a flash device is programmed:

Initialisation – The FPGA connected to the flash is configured with the XJFlash image required for the target board.
Example time: 2.1 s.

Erase – The flash can be erased using one of two algorithms. The basic erase will simply erase all blocks within a defined range (this may be the whole flash or just the space needed for the image to be programmed). The more intelligent erase will use the fact that it is quicker to read the flash than to erase it; as such it reads from each address and only starts erasing if some data is found. This step can be skipped if it is known that the flash will always be blank before it is programmed.
Example time – intelligent erase enabled:
0.9 s with a device already erased, to 23 s with a fully programmed device (limited by erase time of device).

Program – Data from the target images is streamed into the FPGA through its JTAG port. The FPGA then programs this data into the connected flash(s). Multiple files can be specified and programmed at defined offsets. This step can be bypassed if only verification is required.
Example time: 6.2 s (limited by the programming speed of the device).

Verify – The verification checks every byte in the flash against the specified file(s), ensuring there are no data bit errors. This step can be bypassed if only programming or erasing is required.
Example time: 1.8 s with TCK at 10 MHz, reducing to 1.3 s with TCK at 20 MHz.

These example times are provided for a Spartan 6 XC6SLX9 programming a 2 MByte pseudo-random data file into the FPGA's SPI configuration PROM.

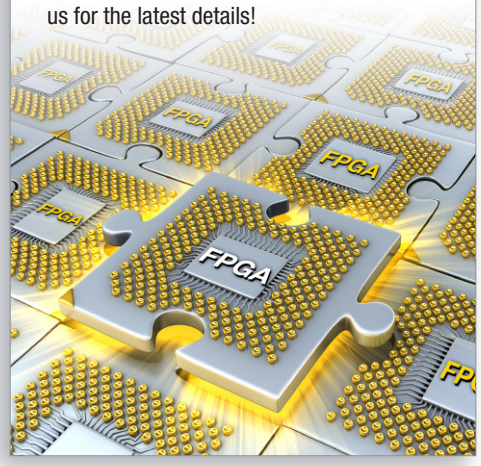
Key Benefits

- Reduce flash programming times
- SPI, QSPI, parallel NOR flash devices supported
- Support for NAND flash devices available on request
- Shortened development cycles
- No need for additional equipment
- Can be used for fast firmware upgrade
- No FPGA development required

Supported FPGAs

- **Intel (Altera)**
  Arria GX, Arria II GX, Arria II GZ, Arria V, Arria V GZ, Arria 10, Cyclone, Cyclone II, Cyclone III, Cyclone III LS, Cyclone IV E, Cyclone IV GX, Cyclone V, Stratix, Stratix GX, Stratix II, Stratix II GX, Stratix III, Stratix IV, Stratix V, Stratix 10
- **Lattice**
  MachXO2, LatticeECP3, LatticeXP2
- **Microchip (Microsemi)**
  IGLOO2, ProASIC3, ProASIC3E, ProASIC3L, SmartFusion2
- **AMD (Xilinx)**
  Artix-7, Artix UltraScale+, Kintex-7, Kintex UltraScale, Kintex UltraScale+, Spartan-3, Spartan-3A, Spartan-3E, Spartan-6, Spartan-7, Versal, Virtex-II, Virtex-II Pro, Virtex-4, Virtex-5, Virtex-6, Virtex-7, Virtex UltraScale, Virtex UltraScale+, Zynq-7000, Zynq UltraScale+

This list is continuously growing, so contact us for the latest details!

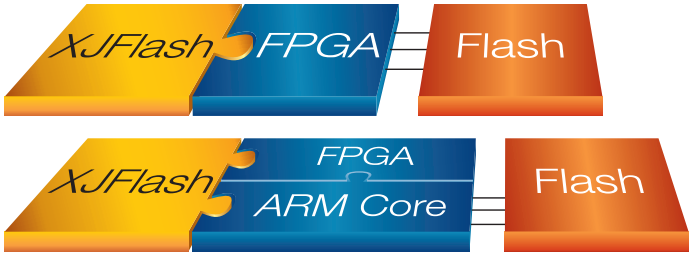


XJFlash

Can I use XJFlash?

In order to use XJFlash, all of the data, address and control signals on the flash device(s) must be connected to an FPGA on the target board. This can be a configuration PROM, or a flash device connected to any general purpose I/O pin. These connections can be direct, indirect, dedicated or shared:

DIRECT CONNECTIONS – YES

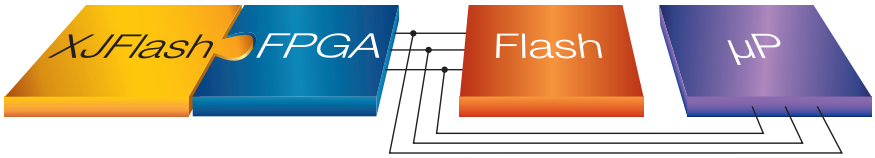


The flash is directly connected to the FPGA.

INDIRECT CONNECTIONS – YES

1. The flash is connected to the FPGA via a buffer.
2. Some of the address signals are shared with the data signals and connected via a latch.
3. There is another configurable device, such as a CPLD between the flash and the FPGA.

SHARED CONNECTIONS – YES



The flash is connected to the FPGA in one of the modes described above but these connections are shared with another device (such as a processor).

NO CONNECTIONS – YES (with design changes)

If your design contains an FPGA but the flash is not connected in any of the configurations described, it may be possible to use spare pins on the FPGA to establish connections to the flash. These connections would not be used in the mission mode of the board but would allow you to use XJFlash to perform fast flash programming. If your FPGA is already connected to the same address/data bus as the flash then this may not require many extra signals.

NO FPGA – Not directly

Unfortunately, it is not possible to use XJFlash if there is no FPGA, but it may be possible to do fast flash programming using the debug interface on a processor – please contact us see if you can use this approach on your board. Alternatively, if it is possible to bring the connections of the flash to a header on the board, XJFlash fast programming can be performed directly via that connector.

Test Integration

XJFlash is fully compatible with the rest of the XJTAG development system. All XJFlash programming can be run as part of an XJRunner boundary scan test project.

Configurable Flash Programming

It doesn't matter whether you need to program a single flash device, or multiple devices that are connected in series, to expand the address space, or in parallel, to make a wider data bus, you can use XJFlash to speed up your programming operations.

Custom Development

XJFlash can also be used for standalone programming requirements including direct access to I^2C and SPI busses or custom protocols such as Microchips ICSP.

The required connections do not need to come from an FPGA on the target board. Providing the protocol signals are available on a header on that board, it should be possible to use XJFlash to achieve fast programming as part of an XJTAG solution.

Please contact us for more details of this service.

Distributor / Technology Partner

XJLink2

Overview

The XJLink2 is a small, portable, USB 2.0 to JTAG controller that provides a high speed interface to the JTAG chain.

The small, lightweight design means the XJLink2 can easily be moved to the Unit Under Test (UUT), while a number of advanced features make it easy to connect to a wide range of circuit boards.

Configurable JTAG interface

Because there is no standard JTAG header or pinout, the XJLink2's JTAG connector is configurable in software to allow you to select the pinout that best suits the board being tested. Two of the connector's 20 pins are fixed grounds (pins 10 and 20), but the JTAG signals for up to four chains can be distributed across the other pins as needed, with any spare pins assignable as digital I/O.

Advanced connectivity

The XJLink2 has variable signal termination, so it can handle boards both with and without signal termination. The advanced auto-skew control enables you to get the maximum frequency out of your JTAG chain and cable while the configurable voltage levels allow you to connect directly to most TAPs.

*Available in black and yellow.**

Your test system where you want it

The XJLink2 contains the license for your XJTAG system. This allows you to easily move your licenses around on and off site to give you maximum flexibility. This also means you aren't tied to one machine to do your XJTAG testing.

Light & portable

The XJLink2 can work with a laptop PC with a USB port and can supply power to low-power target systems, so testing can be done even without a source of mains power. This is especially useful if testing has to be done in the field or in a very busy lab.

**Subject to availability.*

Key Benefits

- Small, lightweight, portable design: ideal for lab and field work
- Self-contained licence allowing you to use the XJTAG system on multiple machines
- Re-configurable unit for multiple UUTs saving costs

Features

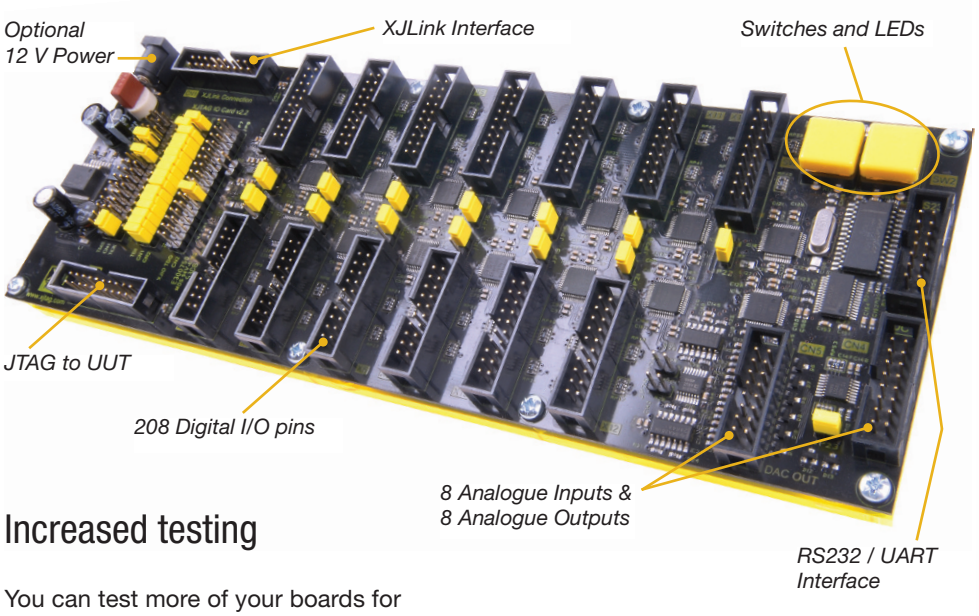
- Up to 4 TAP connections to UUT
- Configurable JTAG connector pinout to suit DUT
- USB bus-powered (no external PSU)
- TCK clock frequencies up to 166 MHz
- Two different voltages can be configured, from 1.1 V to 3.3 V in 0.1 V steps
- Button to start test
- Visual indication of test status
- High speed USB 2.0 interface, backwards compatible with USB 1.0 & 1.1
- Adjustable JTAG signal termination
- Spare pins on the JTAG connector can be used in place of the button or to indicate the test status
- Pins can also be used as general purpose I/O during testing, for example for fast Flash programming
- Automatic signal skew control
- Can supply power to the target board (3.3 V, <100 mA)
- Built in voltage meter on all I/O pins
  Voltage input: Min 0, Max 5 V
- Frequency counter on all I/O pins
  Frequency input: Min 1 Hz, Max 200 MHz
  Selectable measurement period of 1ms, 10ms, 100ms, 1s, 10s
- JTAG signals are +5 V tolerant

XJIO Board

Overview

The XJIO board is an expansion unit that will integrate with your XJTAG test system to provide access to otherwise inaccessible areas of your circuit.

With a range of digital and analogue I/O on the XJIO board, you can increase test coverage and improve fault isolation.



Increased testing

You can test more of your boards for opens and shorts by connecting signals from your Unit Under Test (UUT) to the XJIO board.

Although often overlooked in test, connectors are a common source of manufacturing faults, especially with the increased use of high density connectors. By adding an XJIO board to your test system, XJTAG can drive signals through your connectors and identify the nature and location of any faults.

With onboard DAC and ADC the XJIO board provides a mechanism for analogue as well as digital testing. Using this functionality, even boards with no JTAG components can be "black box" tested with XJTAG.

Digital interface

With 208 bidirectional digital I/O pins, the XJIO board has been designed for maximum connectivity. The I/O pins are all 5 V tolerant. The default logic level is 3.3 V, or you can re-configure the I/O pins, in blocks of 16, to use any user-defined voltage between 3.3 V and 1.8 V.

Analogue interface

The XJIO board has 8 analogue inputs and 8 analogue outputs, controllable via the JTAG interface. The on-board ADC enables analogue measurement —e.g. testing a power rail is within limits. The DAC allows analogue inputs on the UUT to be stimulated, improving test coverage of the target board.

RS232 interface

This interface can be used to further improve test coverage. There is a UART capable of communication up to 230 kbit/s and a RS232 transceiver that can be driven directly from the JTAG chain.

Power supplies

For quick and portable test setup the XJIO board can be powered from USB. Alternatively, if you need more than 80 mA of current, there is a connector for a standard 12 V power supply.

Key Benefits

- Improve reliability of your boards by increasing analogue and digital test coverage
- Reduce your debug time by enhanced fault isolation
- XJTAG can reduce the cost and complexity of your custom test jigs
- Reach devices on your non-JTAG boards with "black box" testing

Features

- Configure the voltage of the 208 digital I/O pins –1.8 V to 3.3 V (5 V tolerant)
- On-board 8 channel ADC and DAC
- Fully expandable to meet your needs
- Switches and LEDs for user interaction
- 'Black box' testing for non-JTAG boards
- Reusable, replacing multiple custom test jigs
- Standard IDC connectors
- USB or 12 V power supply
- RS232 / UART

User interaction

The switches and LEDs give further flexibility by providing you with a way to interact with your test system.

Expandable

If more I/O pins are required, XJIO boards can be daisy-chained together via the reconfigurable external JTAG connector to reach the required capacity. All the connectors on the XJIO board are standard IDC, for economical and efficient cable assemblies.

Integration

You can use the XJIO board with any JTAG controller.

FREE HANDS-ON WEBINAR

Fast & easy PCBA hardware testing using XJTAG Boundary Scan

Learn how to setup and run diagnostic tests from your PC without requiring physical access or custom functional test development.

You'll use XJTAG's tools on a remote machine connected to real hardware.

Live Online Workshop

SIGN UP TODAY!

xjtag.com/webinars

Places are limited so book early!